IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

ISSCC®

UNIVERSITY OF PENNSYLVANIA

2024 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 18, 19, 20, 21, 22

CONFERENCE THEME:

ICs For a Better World

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR!
Exhibition
Corporations & Research Institutions

THURSDAY ALL-DAY

4 FORUMS: Analog Circuits; Intelligent Sensing; Frequency Synthesis; Highly-Integrated Transceivers

SHORT-COURSE: Machine Learning Hardware

SUNDAY ALL-DAY

2 FORUMS: Efficient Chiplets and Die-to-Die Communications; Energy-Efficient AI-Computing Systems for Large-Language Models

10 TUTORIALS: Scalable Low-Power Amps; Digitally-Assisted Voltage; Circuit Design 2.5D/3D; Power Management; PLL Techniques; Circuits for Resilience Side Channel; CT ADCs; 3D Flash Memory; Domain-Specific Accelerators; Transceivers for Comm/Sensing

2 EVENING EVENTS: Graduate Student Research in Progress; Mentoring / Networking Session

5-DAY PROGRAM

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 18th, the day before the official opening of the Conference, ISSCC 2024 offers:

- A choice of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums:

  "Efficient Chiplets and Die-to-Die Communications"
  *"Energy-Efficient AI-Computing Systems for Large-Language Models***"**

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday, February 18th, there are two events: "Mentoring Session / Networking Bingo" will be offered starting at 4:00 pm. In addition, the Student-Research Preview, featuring ninety-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 8:00 pm. The SRP will start with an inspirational lecture by Dr. Ian Young (Intel).

On Monday, February 19th, ISSCC 2024 at 8:30 am offers four plenary papers on the theme: "*ICs for a Better World"*. On Monday at 1:30 pm, there are five parallel technical sessions, followed by a Social Hour at 5:30 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers: *"Career Trajectories: Sharing our Paths to Success"*, and *"Mixed Foundry Chiplets? Opportunities and Challenges".*

On Tuesday, February 20th , there are five parallel technical sessions, both morning and afternoon. Book Displays and Author Interviews will be accompanied by a second Demonstration Session. Tuesday evening includes two events, entitled: *"Generative AI for Chip Design"* and "*The Legacy of Gordon Moore".*

On Wednesday, February 21st , there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 22nd, ISSCC offers a choice of five all-day events:

- A Short Course entitled:
  "Machine Learning Hardware: Considerations and Accelerator Approaches"
- Four Advanced-Circuit-Design Forums entitled:
  "*Digitally Enhanced Analog Circuits: Trends & State-of-the-Art Designs"*
  "*Intelligent Sensing"*
  "Recent Developments in High-Performance Frequency Synthesis Circuits and Systems"
  "Toward Next Generation of Highly Integrated Electrical and Optical Transceivers"

This year, again, there is an option that allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

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ISSCC 2024 Circuit Insights

Organizer/Moderator:
Ali Sheikholeslami, *University of Toronto, Toronto, Canada*
ISSCC Education Chair

ISSCC 2024 offers the third edition of its Circuit Insights on Saturday, Feb. 17, 2024, 9:00am - 4:00pm PST. As in the past two years, this event is targeting 3rd- and 4th-year undergraduate students and starting graduate students in the area of circuit design but may be of interest to new circuit design engineers as well. The event will be held in person for a small audience of 50 students (by invitation only) at the ISSCC venue at the Marriott Hotel in San Francisco, and will be recorded for later release on the SSCS/ISSCC YouTube channel.

The event consists of four 60-minute talks on fundamentals of Circuit Design, each to be followed by a 15-minute Q&A Session, with a 1-hour networking lunch after the second talk.

Agenda

Time	Topic
8:30 AM	Coffee
9:00 AM	**Opening Remarks** **Ali Sheikholeslami,** *Circuit Insights Organizer/Moderator*
9:05 AM	**Welcoming Remarks** **Eugenio Cantatore,** *ISSCC Conference Chair* **John Long,** *SSCS President*
9:15 AM	**Fundamentals of Digital Circuit Design** **Jan Rabaey,** *University of California, Berkeley, CA*
10:15 AM	Interactive Q & A
10:30 AM	Break
10:45 AM	**CMOS Circuits for Biomedical Applications** **Carolina Mora-Lopez,** *imec, Leuven, Belgium*
11:45 AM	Interactive Q & A
12:00 PM	Networking Lunch
1:00 PM	**The Basics of Radio Frequency (RF) Circuits** **Hossein Hashemi,** *University of Southern California, CA*
2:00 PM	Interactive Q & A
2:15 PM	Break
2:30 PM	**The Basics of Silicon-Photonic Circuits** **Sudip Shehkar,** *University of British Columbia, Canada*
3:30 PM	Interactive Q & A
3:45 PM	Attendees Feedback/Quiz
4:00 PM	Conclusion

8:30 AM
T1: Process-Scalable Low-Power Amplifiers
Minkyu Je
KAIST, Daejeon, Korea

Dynamic amplifiers have received increasing interest in state-of-the-art systems due to their superior power efficiency and scalability with technology. They have, for example, found many applications in low-power ADCs as error/residue amplifiers or loop filters. This tutorial will introduce various types of dynamic and ring amplifiers. Their conventional structures and basic operational principles will be explained, and a diverse range of topologies, as well as corresponding design tradeoffs, will be described. The effects of PVT variations on their performance and design considerations will also be discussed. Through this tutorial, attendees will obtain a solid understanding of the basics of dynamic and ring amplifiers, including design choices, tradeoffs, and considerations, along with an overview of recent developments.

Minkyu Je received the B.S., M.S., and Ph.D. degrees from KAIST, Korea. He is now an Associate Professor in the School of Electrical Engineering at KAIST, Korea. His research areas are circuits for sensor interfaces, wireless communication, and power management, as well as microsystem integration. He is an editor of 1 book, an author of 6 book chapters, and has more than 300 peer-reviewed international conference and journal publications. He also has more than 50 patents issued or filed. He has served on the TPC for ISSCC, SOVC, and A-SSCC. He was a Distinguished Lecturer of the CASS.

8:30 AM
T2: Fundamentals of Digital and Digitally Assisted Linear Voltage Regulators

Arijit Raychowdhury
Georgia Institute of Technology, Atlanta, GA

Linear voltage regulators, including low-dropout (LDO) regulators, are a popular choice for on-die voltage regulation in SoC processors. Although analog LDOs have been used in supply-sensitive applications over the years, there has been a recent resurgence in research and development of all-digital and digitally assisted LDOs targeted for digital applications. In some of these topologies, traditional design metrics such as power-supply rejection or load regulation are often traded-off for higher energy efficiency and performance during large current and voltage transients, as well as a wide dynamic operating range. This tutorial introduces the fundamentals of all-digital and digitally assisted LDOs and then presents recent advances in circuit topologies. While highlighting the trade-offs between digital and analog LDOs, this presentation covers key metrics such as the transient response, current efficiency, dropout-voltage requirements, and stability via analysis of theoretical control models. Finally, this tutorial explores circuit topologies to unify voltage and clock frequency regulation, to allow designers to reduce voltage guardbands in digital circuits.

Arijit Raychowdhury is the Steve W. Chaddick School Chair in the School of Electrical and Computer Engineering (ECE) at Georgia Tech. He is currently the director of the Center for the Co-Design of Cognitive Systems (CoCoSys), a Joint University Microelectronics Program 2.0. Prior to joining Georgia Tech, Raychowdhury held research positions at Intel Corporation for six years and at Texas Instruments for one-and-a-half years. His research interests include low-power digital and mixed-signal circuit design, design of specialized accelerators, power converters, signal processors, and exploring the interactions of circuits with device technologies. He has published over 350 peer-reviewed articles. He and his students have over 16 best-paper awards and several research awards and fellowships. Raychowdhury is a Fellow of IEEE.

T3: Fundamentals of Circuit Design
for 2.5D/3D Integration

Kenny C. H. Hsieh
TSMC, Hsinchu, Taiwan

Chiplets and 2.5D/3D integration schemes allow performance and yield beyond monolithic approaches. This tutorial covers advanced packaging technologies and the new capabilities they enable. Circuit techniques suitable for side-by-side and stacked integration will be reviewed, including mitigation of inter-symbol-interferences, timing alignment between data and forwarded clocks, shielding against crosstalk, and integrity of power-delivery networks. An example system achieving throughput of 11Tb/s along one millimeter die edge is demonstrated.

Kenny Hsieh is deputy director in TSMC's Design-Technology-Platform organization (DTP) in Hsinchu, Taiwan, where he leads groups responsible for mixed-signal and RF solutions. He joined TSMC in 2013 after working in SerDes design teams at LSI (now Broadcom) and Xilinx (now AMD) in California, USA, for about 15 years in total. Prior to those experiences, Kenny designed SRAM and DRAM. He is now serving on the wireline subcommittee of ISSCC.

T4: Fundamentals of Power Management Systems:
Constraints and Solutions

Frank Praemassing
Infineon Technologies Austria AG, Villach, Austria

Power management systems are partitioned across fine-grained power domains to meet low-power requirements and efficient power-distribution requirements. This tutorial provides an overview of the power-management systems for scalable power domains in modern microcontrollers, including the standby controller subsystem, system startup, power- and clock-generation infrastructure, component monitoring, and power-management integrated-circuit (PMIC) interface. Additionally, concepts are presented to ensure reliable system start-up behavior under demanding power-sequencing conditions.

Frank Praemassing received the Dipl.-Ing. degree in electrical engineering from the University of Bochum, Germany, in 1998. He then continued his PhD studies at the University of Duisburg-Essen and graduated in 2004. Since 2003 he has worked at Infineon in the field of on-chip voltage regulators for MCUs. He is currently Distinguished Engineer with a focus on system resources, which include power- and clock-management, standby controllers, and system-mode management. He is also involved in innovating R&D methodology, particularly in the area of power and signal integrity for mixed-signal analog IP at the SoC and package level.

T5: Calibration Techniques in PLLs

Salvatore Levantino
Politecnico di Milano, Milano, Italy

Digitally assisted PLLs have become the mainstream solution to design lower jitter and more agile clock generators in modern CMOS processes. In this tutorial, after introducing the basics of adaptive filtering, we describe some of the calibration techniques for low-jitter fast-switching frequency synthesizers. These include techniques to correct for digital-time-converter (DTC) gain errors and nonlinearity, to calibrate loop bandwidth, and to speed up lock transients. The tutorial will discuss the issues in the practical implementation of the different approaches and present some state-of-the-art examples.

Salvatore Levantino is a professor at Politecnico di Milano, Italy. He co-authored the textbook Integrated Frequency Synthesizers for Wireless Systems, Cambridge University Press, 2007. He is a member of the TPC of the ISSCC and ESSCIRC. He was an IEEE Distinguished Lecturer for the Solid-State Circuits Society in 2018 and 2019, served on the Steering Committee and the TPC for the IEEE RFIC Symposium from 2012 to 2018, as Guest Editor for the IEEE JSSC in 2016, and as an Associate Editor for IEEE TCAS-I in 2014 and 2015 and IEEE TCAS-II in 2012 and 2013.

T6: Recent Circuit Advances for Resilience to Side-Channel Attacks

Shreyas Sen
Purdue University, West Lafayette, IN

Computationally secure cryptographic algorithms, when implemented on physical hardware, leak correlated physical signatures (e.g. power supply current, electromagnetic radiation, acoustic, thermal) which could be utilized to break the crypto engine. Physical-layer countermeasures, guided by understanding of the physical leakage, including circuit-level and layout-level countermeasures promise strong resilience by reducing the physical leakage at the source of the leakage itself. The past decade has seen significant advancements in circuit-level countermeasures, advancing resilience to side-channel attacks. In this tutorial, we will cover the fundamentals of the leakages and how each countermeasure increases resilience, by diving into the working mechanism of each and comparing the pros and cons of these techniques. The tutorial concludes by highlighting the open problems and future needs of this field.

Shreyas Sen is an Elmore Associate Professor of ECE & BME, Purdue University and the Founder and CTO of Ixana. His current research interests span mixed-signal circuits/systems and electromagnetics for the Internet of Bodies (IoB) and Hardware Security. He has authored/co-authored 3 book chapters, over 200 journal and conference papers and has 20 patents granted/pending. Dr. Sen serves as the Director of the Center for Internet of Bodies (C-IoB) at Purdue. His work has been covered by 250+ news releases worldwide, including invited appearances on TEDx Indianapolis, multiple Television shows (CNBC, NASDAQ live) and podcasts. Dr. Sen is a recipient of the 2018 MIT TR35 India Award, 2022 Georgia Tech 40 Under 40 Award, NSF CAREER Award 2020, AFOSR Young Investigator Award 2016, NSF CISE CRII Award 2017, Intel Outstanding Researcher Award 2020, Google Faculty Research Award 2017, Purdue CoE Early Career Research Award 2021, Intel Labs Quality Award 2012 for industry-wide impact on USB-C type, Intel Ph.D. Fellowship 2010, IEEE Microwave Fellowship 2008, GSRC Margarida Jacome Best Research Award 2007, and nine best paper awards including IEEE CICC 2019, 2021 and in IEEE HOST from 2017 to 2020, for four consecutive years. Dr. Sen's work was chosen as one of the top-10 papers in the Hardware Security field (TopPicks 2019). He serves/has served as an Associate Editor for IEEE Solid-State Circuits Letters (SSC-L), Nature Scientific Reports, Frontiers in Electronics, IEEE Design & Test, and as a TPC member of ISSCC, CICC, CCS, DAC, IMS, DATE, ISLPED, ICCAD, among others. Dr. Sen is a Senior Member of IEEE.

1:30 PM
T7: Fundamentals of Continuous-Time ADCs
Shanthi Pavan
IIT Madras, Chennai, India

This tutorial provides a comprehensive overview of continuous-time analog-to-digital converters (ADCs), with a focus on the principles and architectures behind these devices. We start with an introduction to the basics of sampling and quantization, before delving into the operation of continuous-time ADCs. We cover various architectures, including continuous-time pipeline ADCs and continuous-time multistage noise-shaping (MASH) converters, and explain the trade-offs and design considerations for each. The tutorial provides intuitive explanations of the underlying principles, making it accessible to beginners while also providing valuable insights for more experienced designers. By the end of this tutorial, participants will have a solid understanding of continuous-time ADCs and their underlying principles.

Shanthi Pavan is the Alexander Chair Professor of Electrical Engineering at the Indian Institute of Technology, Madras. He is co-author of "Understanding Delta-Sigma Modulators (second edition)" which received the Outstanding Professional Book Award from IEEE Press in 2020. Shanthi has received numerous awards for his work, including the Outstanding Forum Presenter at ISSCC 2021. He serves on the Technical Program Committee (TPC) of ISSCC and on the editorial boards of the IEEE Journal of Solid-State Circuits and Solid-State Circuits Letters. He is a Fellow of the IEEE.

1:30 PM
T8: 3D Flash Memory from Technology to the System: Past, Present and Future Developments
Violante Moschiano
Intel, Rome, Italy

Meeting the increasing demand for non-volatile memory in a range of critical applications has required improving memory cost, performance, and power consumption. Moving from 2D to 3D NAND has become critical for meeting these requirements. Substantial density increase is enabled by wafer-level stacking of more than 300 layers and by multi-level cells via threshold-voltage scaling, with up to 5bits/cell. But, such stacking and threshold-voltage control introduce sensitivities to reliability and variations, which impact overall system performance and must be managed with smart circuit design. This tutorial covers the fundamentals of 3D NAND flash, describing the main blocks and major design approaches that have led to the most recent innovations in the field. The tutorial goes on to describe tradeoffs between the components that impact system operation, with intuition on how component-level metrics (t_{read}, t_{prog}, trigger rate) translate to system requirements (MB/s, IOPS, QoS). The tutorial concludes by overviewing and introducing future trends in flash memory to provide perspectives on the evolution of NAND over the next decade.

Violante Moschiano is a Senior Director and Senior Principal Design Engineer at Intel. He received a master's degree in electronic engineering from the University of Naples "Federico II" (Italy) in 2003. In 2004, he joined Micron Technology (Avezzano, Italy), where he spent 18 years involved in NAND flash memory, contributing to the development of important innovation in the field. Violante has authored over 300 U.S. Patents and Applications, and has published papers in key IEEE conferences. He has served on the ISSCC ITPC in the memory subcommittee since 2020.

T9: Domain-Specific Accelerators:
From Hardware to Systems

Sophia Shao
UC Berkeley, Berkeley, CA

Domain-specific accelerators have become a key component in today's systems-on-chip (SoCs) and systems-on-package (SoPs), driving active research and product development to build novel accelerators for emerging applications such as machine learning, robotics, cryptography, and many more. This tutorial will discuss challenges and opportunities for the next generation of domain-specific accelerators, with a special focus on system-level implications of designing, integrating, and scheduling of future heterogeneous platforms. Specifically, we will cover: hardware optimization for efficient accelerator design; state-of-the-art SoC integration protocols (AXI, TileLink, CXL); and runtime system design to dynamically manage accelerator and shared resources at the system level.

Sophia Shao is an Assistant Professor of EECS at UC Berkeley. Previously, she was a Senior Research Scientist at NVIDIA and received her Ph.D. degree in 2016 from Harvard University. Her research interests are in the area of computer hardware, with a special focus on domain-specific architecture, deep-learning accelerators, and design methodology. Her work has been awarded a Best Paper Award at MICRO'2019, a Best Paper Award at DAC'2021, a Best Paper Award at JSSC'2021, a Research Highlight of CACM (2021), Top Picks in Computer Architecture (2014), and two Honorable Mentions (2019).

3:30 PM

T10: Fundamentals of Transceivers
for Communication and Sensing

Giuseppe Gramegna
imec, Leuven, Belgium

Wireless communication and radar systems are ubiquitous, and integrating both together is an active recent area of research. This tutorial will cover the basics of wireless communication and FMCW/PMCW/OFDM radar, while adopting a unified language and approach to encompass both communication and sensing topics. The advantages and disadvantages of existing transceiver architectures and beamforming implementations for communication and sensing will be explained, while MIMO radar will be introduced and compared with a beamforming approach. A few building blocks common to communication and radar systems will be described. Finally, a communication implementation will be compared with several radar architectures to provide insights into the challenges of adding sensing functionality to a communication system.

Giuseppe Gramegna, MS (1993) and Ph.D (1996), started his career at imec and later worked on low-noise CMOS front-ends and GPS SoCs at STMicroelectronics until 2008. Following that, he held leadership positions at Nemerix, CSR, and Samsung, where he led the development of fully integrated GPS and BT/WiFi chipsets until 2015. He then moved to Huawei, where he contributed to the design of 5G mm-wave Radios. In 2018, he joined RFS as R&D Director. Since 2021, he is at imec, focusing his research on phased-array communication and sensing architectures for 6G. Giuseppe has served on the Technical Program Committee (TPC) for IEEE ESSCIRC from 2005 to 2018 and the TPC for ISSCC (RF sub-committee) from 2017 to 2018. Since 2021, he has been serving on the ISSCC TPC (Wireless sub-committee). He has co-authored numerous papers and patents in the field of communication and sensing architectures.

Efficient Chiplets and Die-to-Die Communications

Organizers:	**Shidhartha Das,** *AMD, Cambridge, United Kingdom* **John Wuu,** *AMD, Fort Collins, CO*
Co-Organizers:	**Yvain Thonnart,** *CEA-List, Grenoble, France* **Hugh Mair,** *MediaTek, Austin, TX*
Champions:	**Fatih Hamzaoglu,** *Intel, Hillsboro, OR* **Kostas Doris,** *NXP, Eindhoven, The Netherlands*

Maturation of 2.xD/3D technologies has triggered a revolution in computing through chiplet-based heterogeneous integration of disparate process technologies and computing architectures. Beyond yield enhancement, the integration of general-purpose computing, domain-specific accelerators and cutting-edge memory technologies enables opportunities for substantial performance and energy-efficiency gains. System modularity drives a greater emphasis on standardized energy-efficient chip-to-chip communication necessitating cross-domain innovations across process technology, system architectures and transceiver design while guaranteeing link performance under adverse power delivery and thermal ambient conditions. This forum will feature expert technologists and architects who will describe the SotA and the future trends for technology, heterogeneous computing architectures and chip-to-chip communications, covering the whole spectrum of challenges from protocol definitions to emerging technologies, circuit design and test.

Agenda

Time	**Topic**
8:00 AM	Breakfast
8:15 AM	**Introduction** **John Wuu,** *AMD, Fort Collins, CO*
8:25 AM	**Advanced CMOS and Packaging Technology for Multi-Chiplet and Trillion Transistor 3DIC System-in-Package by 2030** **Yujun Li,** *TSMC, Hsinchu, Taiwan* **Geoffrey Yeap,** *TSMC, Hsinchu, Taiwan*
9:15 AM	**The Packaging and Interconnect Requirements of the IC Industry's Chiplet-Based Future** **Sam Naffziger,** *AMD, Fort Collins, CO*
10:05 AM	Break
10:20 AM	**Do Chiplets Open the Space for Emerging Memory in the HPC System?** **Sebastien Couet,** *IMEC, Leuven, Belgium* **Gouri Sankar Kar,** *IMEC, Leuven, Belgium*
11:10 AM	**In-Memory Computing Chiplets for Future AI Accelerators** **Echere Iroaga,** *EnCharge AI, Santa Clara, CA*
12:00 PM	Lunch
1:20 PM	**Efficient Domain-Specific Compute with Chiplets** **Dejan Marković,** *UCLA, Los Angeles, CA*
2:10 PM	**Innovations in Chiplet Interconnects, Protocols and the Path to Standardization** **Lihong Cao,** *ASE US, Austin, TX*
3:00 PM	Break
3:15 PM	**Photonics for Die-to-Die Interconnects: Links and Optical I/O Chiplets** **Chen Sun,** *Ayar Labs, Santa Clara, CA*
4:05 PM	**Robust Circuit/Architecture Co-Design for Chiplet Integration** **Wen-Chou Wu,** *MediaTek, Hsinchu, Taiwan*
4:55 PM	Closing Remarks

Energy-Efficient AI-Computing Systems for Large-Language Models

Organizers: **Eric Karl,** *Intel, Portland, OR*
                     Jun-Seok Park, *Samsung Electronics, Gyeonggi-do, Korea*

Co-Organizers: **Jae-sun Seo,** *Cornell Tech, New York, NY*
                     Yongpan Liu, *Tsinghua University, Beijing, China*

Champions: **Vivek De,** *Intel, Hillsboro, OR*
                     Alicia Klinefelter, *NVIDIA, Durham, NC*

Large-language models (LLMs), such as ChatGPT and Bard, recently gained tremendous attention by demonstrating astonishing capabilities in recognizing, summarizing, translating, predicting, and generating text and other content based on extensive knowledge from massive datasets. As LLMs serve as a crucial tool for human-to-machine communication, these models are driving a paradigm shift in the capabilities and possibilities for AI computing. The enormous energy consumption for the LLM training and inference has emerged as the key limitation to future AI computing.

This forum presents the current and next generation circuits, architectures, and systems for high-performance computing (HPC) to address the energy-efficiency challenges associated with LLMs. This includes GPU and HPC systems, cloud server SoCs, accelerators, high-bandwidth access to storage, in-package high-bandwidth memory, and DRAM processing in memory. Furthermore, this forum explores LLM quantization techniques to enable next-generation mobile SoCs for LLM inference. This forum welcomes experts across industry and research organizations to present innovations to enable future energy-efficient AI-computing systems for LLMs.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Eric Karl,** *Intel, Portland, OR*
8:25 AM	**A Brief History of Large Language Models…** **and a glimpse into the future** **Larry Heck,** *Georgia Tech, Atlanta, GA*
9:15 AM	**LLM Training and Inference on GPU & HPC Systems** **Mohammad Shoeybi,** *NVIDIA, Santa Clara, CA*
10:05 AM	Break
10:20 AM	**Cloud Processors for LLM Inference** **Sailesh Kottapalli,** *Intel, Santa Clara, CA*
11:10 AM	**LLMs Energy Problem (and what we can do about it)** **Sushma Prasad,** *Google, Sunnyvale, CA*
12:00 PM	Lunch

1:20 PM	**Latency Processing Unit for Acceleration of Large-Language-**
	   Model Inference
	Joo-Young Kim, *KAIST, Daejeon, Korea*
	                    HyperAccel, Gyeonggi-do, Korea

2:10 PM	**High-Bandwidth Memory and Processing-in-Memory in the Era** **of Generative AI** **Kyomin Sohn,** *Samsung, Hwaseong, Korea*
3:00 PM	Break
3:15 PM	**Quantizing LLMs for Efficient Inference at the Edge** **Bram Verhoef,** *Axelera AI, Eindhoven, The Netherlands*
4:05 PM	**Next-Generation Mobile Processors with Large-Language** **Models (LLMs) and Large Multimodal Models (LMMs)** **Bor-Sung Liang,** *MediaTek, Hsinchu City, Taiwan*
4:55 PM	Closing Remarks

Mentoring Session/Networking Bingo Event
(Open to all Attendees)
4:00 - 6:00 PM

Women in Circuits (WiC) together with ISSCC will be holding a networking and mentoring session on Sunday afternoon. Distinguished panelists from the "Sharing Our Paths to Success" panel, WiC members, and other participants will play getting-to-know-you bingo to promote engagement between various members of the community. This will give participants the chance to network and mingle with people across a spectrum of seniority in the field in a casual setting. This event is open to all ISSCC attendees and the public.

EE1:   Student Research Preview (SRP)
8:00 PM

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 23 sixty-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: 1) 5G+, Satcom, Optical and Quantum Circuits, 2) Advances in Power, Data Conversion, and Frequency Synthesis Techniques, and 3) Cutting-edge Processing and Sensing Techniques.

The SRP will include an inspirational lecture by Dr. Ian Young (Intel). SRP begins at 8:00 pm on Sunday, February 18th. It is open to all ISSCC registrants.

SRP Organizing Committee

Co-Chair:	**Jerald Yoo**, *National University of Singapore, Singapore*
Co-Chair:	**Mondira (Mandy) Pant**, *Intel, MA*
Advisor:	**Anantha Chandrakasan**, *Massachusetts Institute of Technology, MA*
Advisor:	**Jan Van der Spiegel**, *University of Pennsylvania, Philadelphia, PA*
Media/Publications:	**Laura Fujino**, *University of Toronto, Toronto, Canada*
A/V:	**Trudy Stetzler**, *Halliburton, Houston, TX*

Committee Members

Utsav Banerjee, *IISC, India*

Po-Hung Chen, *National Chiao Tung University, Taiwan*

Woo-Seok Choi, *Seoul National University, Korea*

Sijun Du, *Delft University of Technology, The Netherlands*

Antoine Frappé, *University of Lille, France*

Hao Gao, *Eindhoven University of Technology, The Netherlands*

Preet Garcha, *Texas Instruments, TX*

Minkyu Je, *KAIST, Korea*

Matthias Kuhl, *University of Freiburg, Germany*

Jaydeep Kulkarni, *University of Texas at Austin, TX*

Jiamin Li, *Southern University of Science and Technology, China*

Xilin Liu, *University of Toronto, Toronto, Canada*

Noriyuki Miura, *Osaka University, Japan*

Phillip Nadeau, *Analog Devices, MA*

Mondira Pant, *Intel, MA*

Negar Reiskarimian, *Massachusetts Institute of Technology, MA*

Chutham Sawigun, *imec, Belgium*

Atsushi Shirane, *Tokyo Institute of Technology, Japan*

Mahsa Shoaran, *EPFL, Switzerland*

Yildiz Sinangil, *Apple, CA*

Mahmut Sinangil, *Nvidia, CA*

Filip Tavernier, *KU Leuven, Belgium*

Chia-Hsiang Yang, *National Taiwan University, Taiwan*

Lita Yang, *Meta, CA*

Rabia Tugce Yazicigil, *Boston University, MA*

Jerald Yoo, *National University of Singapore, Singapore*

Milin Zhang, *Tsinghua University, China*

Plenary Session — Invited Papers

Chair: **Eugenio Cantatore,** *Eindhoven University of Technology,*
                                        Eindhoven, The Netherlands
                 ISSCC Conference Chair

Associate Chair: **Frank O'Mahony,** *Intel, Hillsboro, OR*
                 ISSCC International Technical-Program Chair

FORMAL OPENING OF THE CONFERENCE   **8:30 AM**

1.1   Semiconductor Industry: Present & Future   8:50 AM

Kevin Zhang, *Senior Vice President, Business Development*
& Overseas Operations Office,
Taiwan Semiconductor Manufacturing Company

Semiconductors are the foundation of today's digital economy and are powering innovations that will shape the trajectory of human history. This paper highlights the latest progress of the semiconductor industry to support a vast spectrum of applications that have forever changed our lives. It gives insight into the paths of continued advanced technology scaling, the essential role of design-technology co-optimization (DTCO), and how system-level integration will elevate system performance to new heights. The advancements of semiconductors will enable many new innovations in artificial intelligence (AI), high-performance computing (HPC), wireless connectivity, and autonomous driving. The paper also provides the trends of technologies ranging from low-power and edge AI devices to cloud-based computing. By harnessing the new capabilities of semiconductors, these innovations will greatly improve productivity, efficiency, safety, as well as sustainability. The semiconductor industry is indeed experiencing a "golden era" in spurring remarkable economic growth and unleashing innovations to create a better future for society.

1.2   Racing Down the Slopes of Moore's Law   9:20 AM

Bram Nauta, *University of Twente, Enschede, The Netherlands.*

Since its inception, Moore's Law has been the driving force for IC design. Although during the first decade, "everything" seemed to be better, however, we lost the scaling of processor clock speed and RF transistor speed, and now it looks as if power efficiency of digital gates will stall. What remains is scaling in transistor count and cost-per-function, thanks to 3D integration.

Thus, this is an excellent moment to reconsider how we design for analog and digital signal processing. The higher the required signal-to-noise ratio (SNR), the more power-efficient digital signal processing is compared to analog. Pure analog processing remains more efficient only for ~30dB SNR or less. In the case of digital processing, the conversion from analog to digital should therefore be made as early in the signal chain as possible. Thanks to the figure-of-merit race, analog-to-digital converters (ADCs) have experienced a tremendous win in power efficiency. However, these ADCs require a large input voltage swing while the input signals to be converted, from an antenna or sensor interface, are usually much smaller. Therefore, RF and analog front-ends are needed, which consume much more power than the ADCs to be driven.

Let us re-think these analog front-ends. Can we still efficiently design these front-ends in future CMOS? Do we need so much linear amplification? Do we need active linear circuits at all? Can we not use "digital" components to replace the analog front-ends and ADCs?

ISSCC, SSCS, IEEE AWARD PRESENTATIONS   **9:50 AM**

BREAK   **10:15 AM**

1.3   Computing in the Era of Generative AI   10:45 AM

Jonah Alben, *Senior Vice President, GPU Engineering*
NVIDIA

Generative AI has captured the imagination of users across multiple industries, and we have only begun to tap the potential of this amazing technology. GenAI applications can create text, computer code, protein sequences, images, video, rendered 3D graphics, music, with more generation types being constantly added. The combination of high compute demands, and the real-time requirements of many GenAI-based applications requires design thinking at data-center scale. This paper will cover the breadth of technology innovations, from circuits to silicon to software to data center, needed to enable today's latest supercomputers for GenAI, and discuss our experiences applying GenAI to various business sectors.

1.4   Fueling Semiconductor Innovation   11:15 AM
         and Entrepreneurship in the Next Decade

Lip-Bu Tan, *Chairman of Walden International,*
                    Founding Managing partner of Walden Catalyst Ventures,
                    Senior Advisor & former CEO Cadence Design

This paper provides a comprehensive overview of the future of semiconductor technology, focusing on the interplay between innovation and entrepreneurship. It is organized into sections that discuss the current state of the semiconductor industry, the role of entrepreneurship in driving innovation, and the potential future developments in this field. It highlights the virtuous cycle of innovation and entrepreneurship, where advancements in semiconductor technology fuel new business opportunities, which in turn drive further technological progress. This cycle is crucial for the creation of the next generation of intelligent electronic systems. The paper also explores the 'stack' of semiconductor technology, from materials and design to manufacturing and generative AI applications. It establishes that there are beneficial relationships between these different parts of the stack, with advancements in one area often enabling progress in others. This interconnectedness underscores the importance of a holistic approach to innovation in the semiconductor industry, where advancements in different parts of the stack can collectively drive the industry forward.

PRESENTATION TO PLENARY SPEAKERS   11:45 AM

CONCLUSION   11:50 AM

Processors and Communication SoCs

Session Chair: **Shidhartha Das,** *Advanced Micro Devices, Cambridge, United Kingdom*
Session Co-Chair: Sugako Otani, *Renesas Electronics, Kodaira, Japan*

1:30 PM

2.1 **A 4nm 3.4GHz Tri-Gear Fully Out-of-Order ARMv9.2 CPU Subsystem-Based 5G Mobile SoC**
A. Varma[1], S. Gururajarao[1], H. Chen[1], T. Chen[1], G. Gammie[1], H. Mair[2], J-H. Yang[3], H-H. Yu[3], S-C. Chang[3], C-H. Yang[3], L-A. Huang[3], K. Ramanathan[1], R. Halli[4], E. Ho[1], T-W. Hung[3], S-Y. Hsueh[3], L. Li[3], A. Thippana[1], E. Wang[3], S. Hwang[3]
[1]MediaTek, Austin, TX; [2]MediaTek, Dallas, TX; [3]MediaTek, Hsinchu, Taiwan
[4]MediaTek, Bengaluru, India

1:55 PM

2.2 **"Zen 4c": The AMD 5nm Area-Optimized x86-64 Microprocessor Core**
T. Burd[1], S. Venkataraman*[1], W. Li*[1], T. Johnson[1], J. Lee[1], S. Velaga[1], M. Wasio[1], T. Yiu[1], F. Bodine[1], M. McCabe[1], U. Salim[1], S. K. Thouta[1], M. Golden[1], S. Ramachandran [1], G. S. L. Devi[1], J. Wuu[2], Y. Kuszczak[3], G. Singla[3], C. Henrion[2], A. Robison[2], S. Balagangadharan[4], U. Nair[4], N. Srivastava[4], H. Prasad[4], M. Polimetla[4], P. Chennupati[4], E. Gupta[4], M. Vykuntam[4], S. Sarkar[4], P. K. Duvvuru[4], T. Mardi[4], S. G[4]; [1]AMD, Santa Clara, CA; [2]AMD, Fort Collins, CO
[3]AMD, Markham, Canada; [4]AMD, Bangalore, India
*Equally Credited Authors (ECAs)

2:20 PM

2.3 **Emerald Rapids: 5th-Generation Intel® Xeon® Scalable Processors**
A. O. Munch[1], N. Nassif[1], C. L. Molnar[1], J. Crop[2], R. Gammack[1], C. P. Joshi[3], G. Zelic[1], K. Munshi[1], M. Huang[4], C. R. Morganti[2], S. Kandula[1], A. Biswas[1]
[1]Intel, Hudson, MA; [2]Intel, Fort Collins, CO; [3]Intel, Hillsboro, OR
[4]Intel, Santa Clara, CA

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2.4 **DS1** **ATOMUS: A 5nm 32TFLOPS/128TOPS ML System-on-Chip for Latency Critical Applications**
C-H. Yu, H-E. Kim, S. Shin, K. Bong, H. Kim, Y. Boo, J. Bae, M. Kwon, K. Charfi, J. Kim, H. Kim, M. Shim, C. Ha, W. Shin, J-S. Yoon, M. Chi, B. Lee, S. Choi, D. Kim, J. Woo, S. Yoon, H. Jo, H. Kim, H. Heo, Y-J. Jin, J. Yu, J. Lee, H. Kim, M. Kang, S. Choi, S-G. Kim, M. Choi, J. Oh, Y. Kim, H. Kim, S. Je, J. Ham, J. Yoon, J. Lee, S. Park, Y. Park, J. Lee, B. Hong, J. Ryu, H. Ko, K. Chung, J. Choi, S. Jung, Y. F. Arthanto, J. Kim, H. Cho, H. Jeong, S. Choi, S. Han, J. Park, K. Lee, S-I. Bae, J. Bang, K-J. Lee, Y. Jang, J. Park, S. Park, J. Park, H. Shin, S. Park, J. Oh, Rebellions, Seongnam-si, Korea

Break 3:10 PM
3:35 PM

2.5 **A 28nm Physical-Based Ray-Tracing Rendering Processor for Photorealistic Augmented Reality with Inverse Rendering and Background Clustering for Mobile Devices**
S. Guo[1], S. Sapatnekar[2], J. Gu[1]
[1]Northwestern University, Evanston, IL; [2]University of Minnesota, Minneapolis, MN

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2.6 **A 131mW 6.4Gb/s 256×32 Multi-User MIMO OTFS Detector for Next-Gen Communication Systems**
T. Lee, T-Y. Chen, I-H. Liu, C-H. Yang, National Taiwan University, Taipei, Taiwan

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2.7 **DS1** **BayesBB: A 9.6Gb/s 1.61ms Configurable All-Message-Passing Baseband-Accelerator for B5G/6G Cell-Free Massive-MIMO in 40nm CMOS**
Y. Zhang *[1,2], W. Zhou *[1,2], Y. Zhang[1,2], H. Ji[1,2], Y. Huang[1,2], X. You[1,2], C. Zhang[1,2]
[1]Southeast University, Nanjing, China
[2]Purple Mountain Laboratories, Nanjing, China
*Equally Credited Authors (ECAs)

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2.8 **A 21.9ns 15.7Gb/s/mm² (128, 15) BOSS FEC Decoder for 5G/6G URLLC Applications**
D. Kam[1], S. Yun[1], J. Choe[1], Z. Zhang[2], N. Lee[3], Y. Lee[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]University of Michigan, Ann Arbor, MI; [3]Korea University, Seoul, Korea

Conclusion 5:15 PM

Analog Techniques

Session Chair:　　**Jiawei Xu,** *Fudan University, Shanghai, China*
Session Co-Chair:　**Jens Anders,** *University of Stuttgart, Stuttgart, Germany*

1:30 PM

3.1 **A PVT-Insensitive Sub-Ranging Current Reference Achieving 11.4ppm/°C**
DS1 **from -20°C to 125°C**
P. Park[1], J. Lee[2], S. Cho[1]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

1:55 PM

3.2 **A 0.028mm² 32MHz RC Frequency Reference in 0.18μm CMOS with**
±900ppm Inaccuracy from –40°C to 125°C and ±1600ppm Inaccuracy
After Accelerated Aging
S. Pan[1], Y. Cheng[1], G. Wu[1], Z. Wang[1], K. A. A. Makinwa[2], H. Wu[1]
[1]Tsinghua University, Beijing, China
[2]Delft University of Technology, Delft, The Netherlands

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3.3 **A 0.5V 6.14μW Trimming-Free Single-XO Dual-Output Frequency**
DS1 **Reference with [5.1nJ, 120μs] XO Startup and [8.1nJ, 200μs]**
Successive-Approximation-Based RTC Calibration
R. Luo[1], K-M. Lei[1], R. P. Martins[1,2], P-I. Mak[1]
[1]University of Macau, Macau, China; [2]University of Lisboa, Lisbon, Portugal

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3.4 **A 14b 98Hz-to-5.9kHz 1.7-to-50.8μW BW/Power Scalable Sensor**
Interface with a Dynamic Bandgap Reference and an Untrimmed Gain
Error of ±0.26% from -40°C to 125°C
Z. Tang *[1], Y. Liu *[1], P. Chen[1], H. Wang[1], X. Yu[2], K. A. A. Makinwa[3], N. N. Tan[1]
[1]Vango Technologies, Hangzhou, China; [2]Zhejiang University, Hangzhou, China
[3]Delft University of Technology, Delft, The Netherlands
*Equally Credited Authors (ECAs)

Break 3:10 PM
3:35 PM

3.5 **A 4mW 45pT/√Hz Magnetoimpedance-Based ΔΣ Magnetometer with**
Background Gain Calibration and Short-Time CDS Techniques
I. Akita[1], S. Tatematsu[2], [1]AIST, Tsukuba, Japan; [2]Aichi Steel, Tokai, Japan

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3.6 **An Amplifier-Less CMOS Potentiostat IC Consuming 3.7nW Power all**
over 129.5dB Dynamic Range for Electrochemical Biosensing
M. A. Akram[1], A. Aberra [1], S-J. Kweon[2], S. Ha[1,3]
[1]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates
[2]The Catholic University of Korea, Bucheon, Korea
[3]New York University, New York, NY

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3.7 **A β-Compensated NPN-Based Temperature Sensor with ±0.1°C (3σ)**
Inaccuracy from -55°C to 125°C and a 200fJ·K² Resolution FoM
N. G. Toth, K. A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

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3.8 **A 0.65V 900μm² BEoL RC-Based Temperature Sensor with ±1°C**
Inaccuracy from -25°C to 125°C
B-S. Lien *, S. L. Liu *, W-L. Lai, Y-C. Lu, Y-C. Peng, K-H. Hsieh
TSMC, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

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3.9 **A 1.2V High-Voltage-Tolerant Bootstrapped Analog Sampler in 12-bit**
SAR ADC Using 3nm GAA's 0.7V Thin-Gate-Oxide Transistor
S. Lee, J. Park, J. Park, S. Lee, J. Lee, Y. Cho, M. Choi, J. Shin
Samsung Electronics, Hwaseong, Korea

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3.10 **A 0.69/0.58-PEF 1.6nW/24nW Capacitively Coupled Chopper**
Instrumentation Amplifier with an Input-Boosted First Stage in
22nm/180nm CMOS
X. Xu *[1], S. Ye *[1], Y. Luan[1], J. Gao[1], J. Li[1], J. Cui[1], H. Zhang[2], R. Huang[1], L. Shen[1],
L. Ye[1,3]
[1]Peking University, Beijing, China
[2]Nano Core Chip Electronic Technology, Hangzhou, China
[3]Advanced Institute of Information Technology of Peking University, Hangzhou, China
*Equally Credited Authors (ECAs)

Conclusion 5:35 PM

High Performance Transceivers and Transmitters for Communication and Ranging

Session Chair: **Alireza Zolfaghari,** *Broadcom, Laguna Hills, CA*
Session Co-Chair: **Yuanjin Zheng,** *Nanyang Technological University, Singapore, Singapore*

1:30 PM

4.1   **A 79.7μW Two-Transceiver Direct-RF 7.875GHz UWB Radar SoC in 40nm**
DS1   **CMOS**

N. Andersen[1], S. Bagga[1], J. A. Michaelsen[1], H. A. Hjortland[1], L. Leene[1], T. Skår[1], E. Stenersen[1], D. T. Wisland[1,2]
[1]Novelda, Oslo, Norway
[2]University of Oslo, Oslo, Norway

1:55 PM

4.2   **A Tri-Band Dual-Concurrent Wi-Fi 802.11be Transceiver Achieving -46dB**
TX/RX EVM Floor at 7.1GHz for a 4K-QAM 320MHz Signal

J. Lee, J. Jang, W. Lee, B. Suh, H. Yoo, B. Park, J. Woo, J. Jang, I. Ryu, H. Han, J. Kim, B. Kang, M. Kang, H. Kang, J. Kang, M. Lee, D. Lee, H. Son, S. Lee, S. Kim, H. Park, S. Lee, J. Bae, H. Kim, J. Lee, S. Yoo
Samsung Electronics, Hwaseong, Korea

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4.3   **A 43mm² Fully Integrated Legacy Cellular and 5G FR1 RF Transceiver**
with 24RX/3TX Supporting Inter-Band 7CA/5CA 4×4 MIMO with 1K-QAM

J. Bae, S. Lee, J. Lee, I. Jo, H. Kim, K. Yoon, T. Kim, J. Lee, M. Lee, J. Lee, J. Jeong, S. Lee, T. Kim, S. Kim, G. Cho, D. Kim, S. Lee, P. Jang, E. Yang, J. Song, G. Park, S-E. Choi, J. Son, W. Ko, J. Kim, S. H. Park, S. Lee, Y. Lee, E. Park, P. Kang, T. Kim, H. Lee, B. Han, J. Lee, J. Lee, S. Yoo
Samsung Electronics, Hwaseong, Korea

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4.4   **A Highly-Integrated 6-Phase Cell-Reused Digital Transmitter Using 1/3**
Duty-Cycle LO Signals for Harmonic Rejection

J. Li[1], Z. Li*[1], Y. Yin[1], C. Yan[1], N. Qi[2], M. Liu[1], H. Xu[1]*
[1]Fudan University, Shanghai, China
[2]Chinese Academy of Sciences, Beijing, China
*Equally Credited Authors (ECAs)

3:00 PM

4.5   **A Reconfigurable, Multi-Channel Quantized-Analog Transmitter with**
<-35dB EVM and <-51dBc ACLR in 22nm FDSOI

J. Zhong[1], K. Vasilakopoulos[2], A. Liscidini[1]
[1]University of Toronto, Toronto, Canada
[2]Analog Devices, Toronto, Canada

Break 3:15 PM

Wireless RF and mm-Wave Receiver Techniques

Session Chair: **Wu-Hsin Chen,** *Qualcomm, San Diego, CA*
Session Co-Chair: **Ho-Jin Song,** *Pohang University of Science and Technology, Pohang, Korea*

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5.1   A 5-to-16GHz Reconfigurable Quadrature Receiver with 50% Duty-Cycle LO and IQ-Leakage Suppression

H. Xu[1,2], J. Bi[1], T. Zou[1], W. He[1], Y. Zeng[1], J. Gu[1], Z. Jiao[1], S. Liu[3], Z. Zhu[3], N. Yan[1,2]
[1]Fudan University, Shanghai, China
[2]Jiashan-Fudan Joint Research Institute, Jiaxing, China
[3]Xidian University, Xi'an, China

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5.2   0.25-to-4GHz Harmonic-Resilient Receiver with Built-In HR at Antenna and BB Achieving +14/+16.5dBm 3rd/5th IB Harmonic B1dB

S. Araei, S. Mohin, N. Reiskarimian
Massachusetts Institute of Technology, Cambridge, MA

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5.3   A 0.072mm² 18-to-21GHz Non-Uniform Sub-Sampling Receiver with a Non-Uniform Discrete-Time FIR Filter Achieving 42dB Blocker Rejection in 28nm CMOS

M. Ayesh, S. Mahapatra, C. Yang, M-W. Chen
University of Southern California, Los Angeles, CA

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5.4   A 22.4-to-30.7GHz Phased-Array Receiver with Beam-Pattern Null-Steering and Beam-Tracking Techniques Achieving >30.2dB OTA-Tested Spatial Rejection

Y. Yu, B. Sun, M. Geng, C. Zhao, H. Liu, Y. Wu, J. Zhang, K. Kang
University of Electronic Science and Technology of China, Chengdu, China

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5.5   A Stacking Mixer-First Receiver Achieving >20dBm Adjacent-Channel IIP3 Consuming less than 25mW

S. van Zanten, R. van der Zee, B. Nauta
University of Twente, Enschede, The Netherlands

Conclusion 5:30 PM

Imagers and Ultrasound

Session Chair: **Andreas Suess,** *OMNIVISION, San Jose, CA*
Session Co-Chair: **Masaki Sakakibara,** *Sony Semiconductor Solutions Corporation, Atsugi-shi, Kanagawa, Japan*

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6.1 **12Mb/s 4×4 Ultrasound MIMO Relay with Wireless Power and Communication for Neural Interfaces**
E. So, A. Arbabian, Stanford University, Stanford, CA

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6.2 **DS1** **An Ultrasound-Powering TX with a Global Charge-Redistribution Adiabatic Drive Achieving 69% Power Reduction and 53° Maximum Beam Steering Angle for Implantable Applications**
M. Gourdouparis[1,2], C. Shi[1], Y. He[1], S. Stanzione[1], R. Ukropec[3], P. Gijsenbergh[3], V. Rochus[3], N. Van Helleputte[3], W. Serdijn[2], Y-H. Liu[1,2]
[1]imec, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands; [3]imec, Leuven, Belgium

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6.3 **Imager with In-Sensor Event Detection and Morphological Transformations with 2.9pJ/pixel×frame Object Segmentation FOM for Always-On Surveillance in 40nm**
J. Vohra, A. Gupta, M. Alioto, National University of Singapore, Singapore, Singapore

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6.4 **A Resonant High-Voltage Pulser for Battery-Powered Ultrasound Devices**
I. Bellouki[1], N. Rozsa[1], Z-Y. Chang[1], Z. Chen[1], M. Tan[1,2], M. Pertijs[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]SonoSilicon, Hangzhou, China

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6.5 **DS1** **A 0.5°-Resolution Hybrid Dual-Band Ultrasound Imaging SoC for UAV Applications**
J. Guo[1], J. Feng[1], S. Chen[1], L. Wu[1], C-W. Tsai[1,2], Y. Huang[1], B. Lin[1], J. Yoo[1,2]
[1]National University of Singapore, Singapore, Singapore
[2]The N.1 Institute for Health, Singapore, Singapore

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6.6 **Withdrawn by ISSCC**

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6.7 **A 160×120 Flash LiDAR Sensor with Fully Analog-Assisted In-Pixel Histogramming TDC Based on Self-Referenced SAR ADC**
S-H. Han[1], S. Park[1], J-H. Chun[2,3], J. Choi[2,3], S-J. Kim[1]
[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]Sungkyunkwan University, Suwon, Korea; [3]SolidVue, Seongnam, Korea

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6.8 **A 256×192-Pixel 30fps Automotive Direct Time-of-Flight LiDAR Using 8× Current-Integrating-Based TIA, Hybrid Pulse Position/Width Converter, and Intensity/CNN-Guided 3D Inpainting**
C. Zou[1], Y. Ou[1], Y. Zhu[1], R. P. Martins[1,2], C-H. Chan[1], M. Zhang[1]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

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6.9 **A 0.35V 0.367TOPS/W Image Sensor with 3-Layer Optical-Electronic Hybrid Convolutional Neural Network**
X. Wang*, Z. Huang*, T. Liu, W. Shi, H. Chen, M. Zhang
Tsinghua University, Beijing, China; *Equally Credited Authors (ECAs)

5:05 PM

6.10 **A 1/1.56-inch 50Mpixel CMOS Image Sensor with 0.5µm pitch Quad Photodiode Separated by Front Deep Trench Isolation**
D. Kim, K. Cho, H-C. Ji, M. Kim, J. Kim, T. Kim, S. Seo, D. Im, Y-N. Lee, J. Choi, S. Yoon, I. Noh, J. Kim, K. J. Lee, H. Jung, J. Shin, H. Hur, K. E. Chang, I. Cho, K. Woo, B. S. Moon, J. Kim, Y. Ahn, D. Sim, S. Park, W. Lee, K. Kim, C. K. Chang, H. Yoon, J. Kim, S-I. Kim, H. Kim, C-R. Moon, J. Song
Samsung Semiconductor, Hwaseong, Korea

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6.11 **DS1** **A 320x240 CMOS LiDAR Sensor with 6-Transistor nMOS-Only SPAD Analog Front-End and Area-Efficient Priority Histogram Memory**
M. Kim*[1], H. Seo*[1,2], S. Kim[1], J-H. Chun[1,2], S-J. Kim[3], J. Choi[1,2]
[1]Sungkyunkwan University, Suwon, Korea; [2]SolidVue, Seongnam, Korea
[3]Ulsan National Institute of Science and Technology, Ulsan, Korea
*Equally Credited Authors (ECAs)

Conclusion 5:35 PM

Ultra-High-Speed Wireline

Session Chair: **Didem Turker Melek**, *Cadence, San Jose, CA*
Session Co-Chair: **Masum Hossain**, *Carleton University, Ottawa, Canada*

1:30 PM

7.1   A 2.69pJ/b 212Gb/s DSP-Based PAM-4 Transceiver for Optical Direct-Detect Application in 5nm FinFET

J. Q. Wang[1], A. Tan[1], A. Iyer[1], A. Fan[2], A. Farhoodfar[1], B. Alnabulsi[3], B. Smith[3], C. Loi[4], C. R. Ho[1], D. Cartina[5], J. Riani[1], J. Casanova[1], K. Raviprakash[1], L. Patra[1], L. Wang[1], M. Bachu[1], S. Ray[1], S. Chong[4], S. Dallaire[3], T. Nguyen[1], T-F. Wu[2], V. Giridharan[1], V. Gurumoorthy[1], X. Ding[4], Y. Yin[1], Z. Sun[4], S. Jantzi[2], L. Tse[1]
[1]Marvell, Santa Clara, CA; [2]Marvell, Irvine, CA; [3]Marvell, Ottawa, Canada
[4]Marvell, Singapore, Singapore; [5]Marvell, Burnaby, Canada

1:55 PM

7.2 DS1   A 224Gb/s sub-pJ/b PAM-4 and PAM-6 DAC-Based Transmitter in 3nm FinFET

M. Cusmai[1], N. Familia[1], E. Kuperberg[1], M. Nashash[1], D. Gottesman[1], D. Kumar[2], Z. Marcus[1], Y. Horwitz[1], S. Zalcman[1], J. Kim[3], S. Kundu[3], I. Radashkevich[1], Y. Segal[1], D. Lazar[1], U. Virobnik[1], M. P. Li[4], A. Cohen[1]
[1]Intel, Jerusalem, Israel; [2]Intel, Bangalore, India; [3]Intel, Hillsboro, OR
[4]Intel, San Jose, CA

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7.3 DS1   A 224Gb/s 3pJ/b 40dB Insertion Loss Transceiver in 3nm FinFET CMOS

D. Pfaff[1], M. Nummer[1], N. Hai[2], P. Xia[2], K. G. Yang[2], M-M. Mohsenpour[1], M-A. LaCroix[1], B. Zamanlooy[3], T. Eeckelaert[1], D. Petrov[1], M. Haroun[1], C. Dick[2], A. Zaman[1], H. Mei[1], S. Moazzeni[1], T. Shakir[1], C. Carvalho[1], H. Huang[1], P. Kumari[1], R. Mason[1], F. Brishty[2], I. Jaffri[2]
[1]Synopsys, Ottawa, Canada; [2]Synopsys, Mississauga, Canada
[3]Synopsys, Markham, Canada

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7.4   A 0.027mm^2 5.6-to-7.8GHz Ring-Oscillator-Based Ping-Pong Sampling PLL Scoring 220.3fs$_{rms}$ Jitter and −74.2dBc Reference Spur

Y. Huang[1], Y. Chen[1], Z. Yang[2], R. P. Martins[1,3], P-I. Mak[1]
[1]University of Macau, Macau, China
[2]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[3]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Break 3:10 PM
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7.5   A 224Gb/s/wire Single-Ended PAM-4 Transceiver Front-End with 29dB Equalization for 800GbE/1.6TbE

X. Luo[1], X. You[1], Z. Li[1], H. Mosalam[1], D. Xu[1], T. Fan[1], H. Qiao[1], W. Zhou[1], H. Wu[1], L. Zhong[1], P. Y. Chiang[2], Q. Pan[1]
[1]Southern University of Science and Technology, Shenzhen, China
[2]Fudan University, Shanghai, China

4:00 PM

7.6   A 112Gb/s/pin Single-Ended Crosstalk-Cancellation Transceiver with 31dB Loss Compensation in 28nm CMOS

L. Zhong*, H. Wu*, Y. Zhang*, X. Cheng, W. Wu, C. Wang, X. Luo, T. Fan, D. Xu, Q. Pan, Southern University of Science and Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

4:25 PM

7.7 DS1   A 2.16pJ/b 112Gb/s PAM-4 Transceiver with Time-Interleaved 2b/3b ADCs and Unbalanced Baud-Rate CDR for XSR Applications in 28nm CMOS

Y-P. Lin*, P-J. Peng*, C-C. Lu, P-T. Shen, Y-C. Jao, P-H. Hsieh
National Tsing Hua University, Hsinchu, Taiwan; *Equally Credited Authors (ECAs)

4:50 PM

7.8   A 69.3fs Ring-Based Sampling-PLL Achieving 6.8GHz-to-14GHz and -54.4dBc Spurs Under 50mV Supply Noise

M. A. Khalil, M. B. Younis, R. Xia, A. E. Abdelrahman, T. Wang, K-S. Park, P. K. Hanumolu, University of Illinois, Urbana, IL

5:05 PM

7.9   An 8b 6-to-12GHz 0.18mW/GHz DC Modulated Ramp-Based Phase Interpolator in 65nm CMOS Process

S. Mohapatra, E. Afshar, Z. Zhou, D. Heo, Washington State University, Pullman, WA

Conclusion 5:20 PM

Demonstration Session 1, Monday February 19th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 19th, and Tuesday February 20th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2024, as noted by the symbol **DS1**

2.4 ATOMUS: A 5nm 32TFLOPS/128TOPS ML System-on-Chip for Latency Critical Applications

2.7 BayesBB: A 9.6Gb/s 1.61ms Configurable All-Message-Passing Baseband-Accelerator for B5G/6G Cell-Free Massive-MIMO in 40nm CMOS

3.1 A PVT-Insensitive Sub-Ranging Current Reference Achieving 11.4ppm/°C from -20°C to 125°C

3.3 A 0.5V 6.14µW Trimming-Free Single-XO Dual-Output Frequency Reference with [5.1nJ, 120µs] XO Startup and [8.1nJ, 200µs] Successive-Approximation-Based RTC Calibration

4.1 A 79.7µW Two-Transceiver Direct-RF 7.875GHz UWB Radar SoC in 40nm CMOS

6.2 An Ultrasound-Powering TX with a Global Charge-Redistribution Adiabatic Drive Achieving 69% Power Reduction and 53° Maximum Beam Steering Angle for Implantable Applications

6.5 A 0.5°-Resolution Hybrid Dual-Band Ultrasound Imaging SoC for UAV Applications

6.11 A 320x240 CMOS LiDAR Sensor with 6-Transistor nMOS-Only SPAD Analog Front-End and Area-Efficient Priority Histogram Memory

7.2 A 224Gb/s sub-pJ/b PAM-4 and PAM-6 DAC-Based Transmitter in 3nm FinFET

7.3 A 224Gb/s 3pJ/b 40dB Insertion Loss Transceiver in 3nm FinFET CMOS

7.7 A 2.16pJ/b 112Gb/s PAM-4 Transceiver with Time-Interleaved 2b/3b ADCs and Unbalanced Baud-Rate CDR for XSR Applications in 28nm CMOS

8.6 An Integrated Dual-side Series/Parallel Piezoelectric Resonator-Based 20-to-2.2V DC-DC Converter Achieving a 310% Loss Reduction

9.8 A 9.3nV/rtHz 20b 40MS/s 94.2dB DR Signal-Chain Friendly Precision SAR Converter

10.7 An 11GHz 2nd-order DPD FMCW Chirp Generator with 0.051% rms Frequency Error under a 2.3GHz Chirp Bandwidth, 2.3GHz/µs Slope, and 50ns Idle Time in 65nm CMOS

11.3 Metis AIPU: A 12nm 15TOPS/W 209.6TOPS SoC for Cost- and Energy-Efficient Inference at the Edge

11.4 IBM NorthPole: An Architecture for Neural Network Inference with a 12nm Chip

12.3 A Scalable and Instantaneously Wideband 5GS/s RF Correlator Based on Charge Thresholding Achieving 8-bit ENOB and 152 TOPS/W Compute Efficiency

13.5 A 64Gb/s/pin PAM4 Single-Ended Transmitter with a Merged Pre-Emphasis Capacitive-Peaking Crosstalk Cancellation Scheme for Memory Interfaces in 28nm CMOS

14.2 Proactive Voltage Droop Mitigation Using Dual-Proportional-Derivative Control Based on Current and Voltage Prediction Applied to a Multicore Processor in 28nm CMOS

14.5 A 12nm Linux-SMP-Capable RISC-V SoC with 14 Accelerator Types, Distributed Hardware Power Management and Flexible NoC-Based Data Orchestration

14.8 KASP: A 96.8% 10-Keyword Accuracy and 1.68µJ/Classification Keyword Spotting and Speaker Verification Processor Using Adaptive Beamforming and Progressive Wake-Up

15.1 A 0.795fJ/b Physically-Unclonable-Function-Protected TCAM for a Software-Defined Networking Switch

16.2 A 28nm 69.4kOPS 4.4µJ/Op Versatile Post-Quantum Crypto-Processor Across Multiple Mathematical Problems

16.5 A Synthesizable Design-Agnostic Timing Fault Injection Monitor Covering 2MHz to 1.26GHz Clocks in 65nm CMOS

16.6 PACTOR: A Variation-Tolerant Probing-Attack Detector for a 2.5Gb/s×4-Channel Chip-to-Chip Interface in 28nm CMOS

16.7 Power and EM Side-Channel-Attack-Resilient AES-128 Core with Round-Aligned Globally-Synchronous-Locally-Asynchronous Operation Based on Tunable Replica Circuits

18.2 A 4×64Gb/s NRZ 1.3pJ/b Co-Packaged and Fiber-Terminated 4-Ch VCSEL-Based Optical Transmitter

Rising Stars 2024 Workshop

Organizers: **Preet Garcha**, TI, Dallas, TX
                       Ulkuhan Guler, WPI, Worcester, MA

Co-Organizers: **Sally Amin**, Apple, Cupertino, CA
                       Dilara Caygara, BU, Boston, MA
                       Vanessa Chen, CMU, Pittsburgh, PA
                       Zeynep Deniz, IBM Research, Yorktown Heights, NY
                       Najme Ebrahimi, University of Florida, Gainesville, FL
                       Dina Eldamak, GUC, Cairo, Egypt
                       Yasemin Engur, EPFL, Lausanne, Switzerland
                       Q. Jane Gu, UC Davis, Davis, CA
                       Soumya Gupta, OSU, Corvallis, OR
                       Ping-Hsuan Hsieh, NTHU, Hsinchu, Taiwan
                       Yaoyao Jia, UT Austin, Austin, TX
                       Elpida Karapepera, University of Washington, Seattle, WA
                       Kwantae Kim, ETH Zürich, Zürich, Switzerland
                       Rabia Yazicigil Kirby, BU, Boston, MA
                       Alicia Klinefelter, NVIDIA, Durham, NC
                       Deeksha Lal, pSemi, Raleigh, NC
                       Shalini Lal, pSemi, Raleigh, NC
                       Fatemeh Marefat, Keysight Technologies, Santa Clara, CA
                       Aishwarya Natarajan, Hewlett Packard Labs, Milpitas, CA
                       Sirma Orguc, MIT, Cambridge, MA
                       Negar Reiskarimian, MIT, Cambridge, MA
                       Kamala R. Sadagopan, Qualcomm, San Diego, CA
                       Farhana Sheikh, Intel, Hillsboro, OR
                       Trudy Stetzler, Houston, TX
                       Alice Wang, UTD, Richardson, TX
                       Miaorong Wang, Tenstorrent, Cambridge, MA
                       Kathy Wilcox, AMD, Boxborough, MA
                       Wanghua Wu, Samsung Semiconductor, San Jose, CA

Advisors: **Anantha Chandrakasan**, MIT, Cambridge, MA
                       Ingrid Verbauwhede, KU Leuven, Leuven, Belgium

The IEEE SSCS Women in Circuits, together with ISSCC, is sponsoring the "Rising Stars 2024 Workshop" for outstanding students and young professionals in Electrical Engineering and Computer Science. We will be selecting 24 bright minds from both academia and industry, with a holistic approach to diversity. The workshop includes a special dinner, keynote from IEEE Fellow Prof. Ingrid Verbauwhede, and a poster session with lightning talks.

Additionally, established members of academia and industry will talk about their unique journeys in a career panel: "Sharing our Paths to Success", touching upon educational choices, research pursuits, skill development, networking, work-life balance, effective transitioning between academia and industry, and more. The panel is open to all ISSCC 2024 attendees and the public.

Panelists: **Xiaolin Lu**, TI, Dallas, TX
                       Kofi Makinwa, TU Delft, Delft, Netherlands
                       Kathleen Philips, imec, Eindhoven, Belgium
                       Heein Yoon, UNIST, Ulsan, Korea

EE2: Career Trajectories: Sharing Our Paths to Success

Organizers: **Preet Garcha**, TI, Dallas, TX
                     Ulkuhan Guler, WPI, Worcester, MA

Co-Organizers: **Dilara Caygara**, BU, Boston, MA
                     Najme Ebrahimi, University of Florida, Gainesville, FL
                     Yasemin Engur, EPFL, Lausanne, Switzerland
                     Soumya Gupta, OSU, Corvallis, OR
                     Elpida Karapepera, University of Washington, Seattle, WA
                     Alicia Klinefelter, NVIDIA, Durham, NC
                     Kamala R. Sadagopan, Qualcomm, San Diego, CA
                     Farhana Sheikh, Intel, Hillsboro, OR
                     Trudy Stetzler, Houston, TX
                     Alice Wang, UTD, Richardson, TX
                     Kathy Wilcox, AMD, Boxborough, MA
                     Wanghua Wu, Samsung Semiconductor, San Jose, CA

Advisors: **Anantha Chandrakasan**, MIT, Cambridge, MA
                     Ingrid Verbauwhede, KU Leuven, Leuven, Belgium

Moderators: **Ulkuhan Guler**, WPI, Worcester, MA
                     Preet Garcha, TI, Dallas, TX

This career panel event aims to provide a broader perspective on the potential career options available in academia and industry. The panelists will share their experiences, including the pivotal decisions they made, obstacles they encountered, and lessons they learned along the way. They will address critical topics such as educational choices, research pursuits, skill development, networking, work-life balance, and effective transitioning between academia and industry. Participants will gain a deeper understanding of the skills, qualifications, and experiences necessary to excel in each domain, enabling them to make more deliberate choices and develop effective career strategies.

Panelists: **Xiaolin Lu**, TI, Dallas, TX
                     Kofi Makinwa, TU Delft, Delft, Netherlands
                     Kathleen Philips, imec, Eindhoven, Belgium
                     Heein Yoon, UNIST, Ulsan, Korea

EE3:   Mixed-Foundry Chiplets? Opportunities and Challenges

Organizer: **Eric Wang,** *TSMC, Hsinchu, Taiwan*

Co-Organizers: **Arijit Raychowdhury,** *Georgia Institute of Technology, Atlanta, GA*
Daniel Morris, *Meta,* Menlo Park, CA
Vito Giannini, *Uhnder, Austin, TX*
Yongpan Liu, *Tsinghua University, Beijing, China*

Moderator: **Bryan Black,** *Chipletz, Spicewood, TX*

One of the advantages of chiplets is the ability to integrate chiplets developed from different manufacturing processes to realize SoCs with optimal performance/$. An I/O chip, for instance, could be built by one foundry, the core processor could be built by another foundry, and then those chips could be put together on a package. With this, there's potential for mixing and matching chiplets from different foundries. To make this happen, many challenges need to be overcome for the industry, including standardized interfaces between chiplets, verification of whole SoCs using chiplets made from different processes, design flows from multiple foundries, and reliability assurance, including thermal and electromagnetic interactions between chiplets. A mixed-foundry chiplet ecosystem will be crucial to facilitate productization of complex systems-on-chiplet.

Panelists: **Lalitha Immaneni,** *Intel, Tempe, AZ*
Subramanian S. Iyer, *CHIPS R&D Office, Los Angeles, CA*
Yujun Li, *TSMC, Hsinchu, Taiwan*
Sam Naffziger, *AMD, Fort Collins, CO*
Cheolmin Park, *Samsung, Hwaseong, Korea*
Boyd Phelps, *Cadence, Hillsboro, OR*
Geert Van der Plas, *imec, Leuven, Belgium*

Hybrid DC-DC Converters

Session Chair:
Xin Zhang, *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Session Co-Chair:
Lin Cheng, *University of Science and Technology of China, Hefei, China*

8:00 AM

8.1   A 94.5%-Peak-Efficiency 3.99W/mm²-Power-Density Single-Inductor Bipolar-Output Converter with a Concise PWM Control for AMOLED Displays
J. Jin[1], W. Xu*[2], L. Cheng[1,2]*
[1]University of Science and Technology of China, Hefei, China
[2]Hefei CLT Microelectronics, Hefei, China; *Equally Credited Authors (ECAs)

8:25 AM

8.2   A 96.9%-Peak-Efficiency Bilaterally-Symmetrical Hybrid Buck-Boost Converter Featuring Seamless Single-Mode Operation, Always-Reduced Inductor Current, and the Use of All CMOS Switches
D-H. Kim, H-S. Kim, Korea Advanced Institute of Science and Technology, Daejeon, Korea

8:50 AM

8.3   A Li-ion-Battery-Input 1-to-6V-Output Bootstrap-Free Hybrid Buck-or-Boost Converter Without RHP Zero Achieving 97.3% Peak Efficiency 6μs Recovery Time and 1.13μs/V DVS Rate
J. Ruan[1], J. Jiang[2], C. Ding[1], K. Yuan[1], K. N. Leung[3], X. Liu[1]
[1]Chinese University of Hong Kong, Shenzhen, China
[2]Southern University of Science and Technology, Shenzhen, China
[3]Chinese University of Hong Kong, Hong Kong, China

9:15 AM

8.4   A Fast-Transient 3-Fine-Level Buck-Boost Hybrid DC-DC Converter with Half-Voltage-Stress on All Switches and 98.2% Peak Efficiency
S. Zhao[1,2], C. Zhan[2], Y. Lu[1], [1]University of Macau, Macau, China
[2]Southern University of Science and Technology, Shenzhen, China

9:30 AM

8.5   A 6nA Fully-Autonomous Triple-Input Hybrid-Inductor-Capacitor Multi-Output Power Management System with Multi-Rail Energy Sharing, All-Rail Cold Startup, and Adaptive Conversion Control for mm-Scale Distributed Systems
X. Liu, A. Agrawal, A. Tanaka, B. Calhoun, University of Virginia, Charlottesville, VA

Break 9:45 AM
10:05 AM

8.6   An Integrated Dual-side Series/Parallel Piezoelectric Resonator-Based
DS1 20-to-2.2V DC-DC Converter Achieving a 310% Loss Reduction
W-C. B. Liu[1], G. Pillonnet[2], P. P. Mercier[1]
[1]University of California, San Diego, CA; [2]CEA-Léti, Grenoble, France

10:30 AM

8.7   A 92.7% Peak Efficiency 12V-to-60V Input to 1.2V Output Hybrid DC-DC Converter Based on a Series-Parallel-Connected Switched Capacitor
H-J. Choi[1], C-H. Lee[1], Y-J. Jeon[1], H. Park[1], J-H. Kim[1], Y-J. Woo[2], J-P. Hong[2], H. Jin[2], S-W. Hong[1], [1]Sogang University, Seoul, Korea; [2]LX Semicon, Seoul, Korea

10:55 AM

8.8   A 97.18% Peak-Efficiency Asymmetrically Implemented Dual-phase (AID) Converter with a full Voltage-Conversion Ratio (VCR) Between 0 and 1
H-J. Park[1], J-M. Cho[1], C-H. Lee[1], Y-J. Oh[1], H. Jeong[1], J-H. Yang[2], J. Lee[2], S-W. Hong[1]
[1]Sogang University, Seoul, Korea; [2]Samsung Electronics, Seoul, Korea

11:20 AM

8.9   A 96.5% Peak Efficiency Duty-Independent DC-DC Step-Up Converter with Low Input-Level Voltage Stress and Mode-Adaptive Inductor Current Reduction
M. Kim[1], W. Jung[1], H. Park[1], J. Song[1,2], Y. Ahn[2], T. Nam[2], Y. Shin[2], Y-J. Woo[2], H-M. Lee[1]
[1]Korea University, Seoul, Korea; [2]LX Semicon, Seoul, Korea

11:35 AM

8.10 A 5V-to-150V Input-Parallel Output-Series Hybrid DC-DC Boost Converter Achieving 76.4mW/mg Power Density and 80% Peak Efficiency
S. Han[1,2], Z. Fang[1], Z. Tong[1], X. Wu[2], H. Jiang[2], T. Ren[2], Y. Lu[1]
[1]University of Macau, Macau, China; [2]Tsinghua University, Beijing, China

11:50 AM

8.11 A 48V-to-5V Buck Converter with Triple EMI Suppression Circuit Meeting CISPR 25 Automotive Standards
Y-H. Kao[1], C-S. Hung[1], H-H. Chang[1], W-C. Huang[1], R-B. Guo[1], H-Y. Tsai[1], K-H. Chen[1], K-L. Zeng[1,2], Y-H. Lin[3], S-R. Lin[3], T-Y. Tsai[3]
[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]Chip-GaN Power Semiconductor, Hsinchu, Taiwan
[3]Realtek Semiconductor, Hsinchu, Taiwan

Conclusion 12:05 PM

Noise-Shaping and SAR ADCs

Session Chair: **Jongwoo Lee,** *Samsung Electronics, Hwaseong-si, Korea*
Session Co-Chair: **Hajime Shibata,** *Analog Devices, Toronto, Canada*

8:00 AM

9.1   A 2mW 70.7dB SNDR 200MS/s Pipelined-SAR ADC with Continuous-Time SAR-Assisted Detect-and-Skip and Open-then-Close Correlated Level Shifting

S. Ye[1], L. Shen[1], J. Gao[1], J. Li[1], Z. Chen[1], X. Xu[1], J. Cui[1], H. Zhang[2], X. Zhang[1], L. Ye[1,3], R. Huang[1]
[1]Peking University, Beijing, China
[2]Nano Core Chip Electronic Technology, Hangzhou, China
[3]Advanced Institute of Information Technology of Peking University, Hangzhou, China

8:25 AM

9.2   A 2.08mW 64.4dB SNDR 400MS/s 12b Pipelined-SAR ADC Using Mismatch and PVT Variation Tolerant Dynamically Biased Ring Amplifier in 8nm

Y. Lim*, J. Lee*, J. Lee, K. Lim, S. Oh, J. Lee, S-U. Kwak
Samsung Electronics, Hwaseong, Korea
*Equally Credited Authors (ECAs)

8:50 AM

9.3   A 71dB SNDR 200MHz BW Interleaved Pipe-SAR ADC with a Shared Residue Integrating Amplifier Achieving 173dB FoMs

X. He, M. Gu, H. Jiang, Y. Zhong, N. Sun, L. Jie, Tsinghua University, Beijing, China

9:15 AM

9.4   A 182.3dB FoM$_s$ 50MS/s Pipelined-SAR ADC Using Cascode Capacitively Degenerated Dynamic Amplifier and MSB Pre-Conversion Technique

Z. Chen[1], L. Shen[1], S. Ye[1], J. Gao[1], J. Li[1], J. Cui[1], X. Xu[1], Y. Luan[1], H. Zhang[2], L. Ye[1,3], R. Huang[1]
[1]Peking University, Beijing, China
[2]Nano Core Chip Electronic Technology, Hangzhou, China
[3]Advanced Institute of Information Technology of Peking University, Hangzhou, China

Break 9:40 AM
10:05 AM

9.5   A 118.5dBA DR 3.3mW Audio ADC with a Class-B Resistor DAC, Non-Overlap DEM and Continuous-Time Quantizer

A. Subramanian, T. Halder, L. V. Tripurari, A. Kannan
Texas Instruments, Bangalore, India

10:30 AM

9.6   A 6th-Order Quadrature CTDSM Using Double-OTA and Quadrature NSSAR with 171.3dB FoMs in 14nm

J. Lee, S-E. Cho, J. Lee, Y. Lim, S. Oh, J. Lee, S-U. Kwak
Samsung Electronics, Hwasung, Korea

10:55 AM

9.7   A 94.3dB SNDR 184dB FoMs 4th-Order Noise-Shaping SAR ADC with Dynamic-Amplifier-Assisted Cascaded Integrator

K-C. Cheng[1], S-J. Chang[1], C-C. Chen[2], S-H. Hung[2]
[1]National Cheng Kung University, Tainan, Taiwan; [2]Upbeat Technology, Taipei, Taiwan

11:20 AM

9.8   A 9.3nV/rtHz 20b 40MS/s 94.2dB DR Signal-Chain Friendly Precision SAR
DS1 Converter

R. Bodnar[1,2], H. Kennedy[1], C. P. Hurrell[1], A. Ahmad[1], M. Vickery[1], L. Smithers[1], W. Buckley[3], M. Dutt[1], P. Delizia[4], D. Hummerston[1], P. Czapor[3]
[1]Analog Devices, Newbury, United Kingdom
[2]University of Southampton, Southampton, United Kingdom
[3]Analog Devices, Limerick, Ireland; [4]now at Vodafone, Newbury, United Kingdom

11:45 AM

9.9   A 2.72fJ/conv 13b 2MS/s SAR ADC Using Dynamic Capacitive Comparator with Wide Input Common Mode

S. Lee, H. Kang, M. Lee
Gwangju Institute of Science and Technology, Gwangju, Korea

Conclusion 12:00 PM

Frequency Synthesis

Session Chair: **Jun Yin,** *University of Macau, Taipa, Macau*
Session Co-Chair: **Yu-Li Hsueh,** *Mediatek, Hsinchu, Taiwan*

8:00 AM

10.1 An 8.75GHz Fractional-N Digital PLL with a Reverse-Concavity Variable-Slope DTC Achieving 57.3fs$_{rms}$ Integrated Jitter and -252.4dB FoM

M. Rossoni*, S. M. Dartizio*, F. Tesolin, G. Castoro, R. Dell'Orto, C. Samori, A. L. Lacaita, S. Levantino, Politecnico di Milano, Milan, Italy
*Equally Credited Authors (ECAs)

8:25 AM

10.2 A 5.5µs-Calibration-Time, Low-Jitter, and Compact-Area Fractional-N Digital PLL Using the Recursive-Least-Squares (RLS) Algorithm

S. Jang*[1,2], M. Chae*[1,2], H. Park*[1,2], C. Hwang[1,2], J. Choi[2]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Seoul National University, Seoul, Korea; *Equally Credited Authors (ECAs)

8:50 AM

10.3 A 7GHz Digital PLL with Cascaded Fractional Divider and Pseudo-Differential DTC Achieving -62.1dBc Fractional Spur and 143.7fs Integrated Jitter

D. Xu, Z. Liu, Y. Kuai, H. Huang, Y. Zhang, Z. Sun, B. Liu, W. Wang, Y. Xiong, J. Qiu, W. Madany, Y. Zhang, A. A. Fadila, A. Shirane, K. Okada
Tokyo Institute of Technology, Tokyo, Japan

9:15 AM

10.4 A 45.5fs-Integrated-Random-Jitter and -75dBc-Integer-Boundary-Spur BiCMOS Fractional-N PLL with Suppression of Fractional, Horn, and Wandering Spurs

M. P. Kennedy[1,2], V. Mazzaro[1,2], S. Tulisi[3], M. Scully[3], N. McDermott[3], J. Breslin[3]
[1]University College Dublin, Dublin, Ireland
[2]Microelectronic Circuits Centre Ireland, Dublin, Ireland
[3]Analog Devices, Limerick, Ireland

9:30 AM

10.5 A 76fs$_{rms}$-Jitter and -65dBc-Fractional-Spur Fractional-N Sampling PLL Using a Nonlinearity-Replication Technique

Y. Shin*[1,2], J. Lee*[1,2], J. Kim*[1,2], Y. Jo[1,2], J. Choi[2]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Seoul National University, Seoul, Korea; *Equally Credited Authors (ECAs)

Break 9:45 AM
10:05 AM

10.6 A 10GHz FMCW Modulator Achieving 680MHz/µs Chirp Slope and 150kHz rms Frequency Error Based on a Digital-PLL with a Non-Uniform Piecewise-Parabolic Digital Predistortion

F. Tesolin*[1], S. M. Dartizio*[1], G. Castoro[1], F. Buccoleri[1], M. Rossoni[1], D. Cherniak[2], C. Samori[1], A. L. Lacaita[1], S. Levantino[1]
[1]Politecnico di Milano, Milan, Italy; [2]Infineon Technologies, Villach, Austria
*Equally Credited Authors (ECAs)

10:30 AM

10.7 An 11GHz 2nd-order DPD FMCW Chirp Generator with 0.051% rms
`DS1` **Frequency Error under a 2.3GHz Chirp Bandwidth, 2.3GHz/µs Slope, and 50ns Idle Time in 65nm CMOS**

X. Wang*[1,2], X. Ma*[3], Y. Fu[1], Y. Zhou[1], A. Li[1], S. Yang[1], X. Wu[1,2], D. Wang[1,2], L. Li[1,2], X. You[1,2]
[1]Southeast University, Nanjing, China; [2]Purple Mountain Laboratories, Nanjing, China
[3]Télécom SudParis, Paris, France; *Equally Credited Authors (ECAs)

10:55 AM

10.8 A 281GHz, -1.5dBm Output-Power CMOS Signal Source Adopting a 46fs$_{rms}$ Jitter D-Band Cascaded Subharmonically Injection-Locked Sub-Sampling PLL with a 274MHz Reference

B-T. Moon[1,2], H-C. Park[2], S-G. Lee[1]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

11:20 AM

10.9 A 23.2-to-26GHz Sub-Sampling PLL Achieving 48.3fs$_{rms}$ Jitter, -253.5dB FoM$_J$, and 0.55µs Locking Time Based on a Function-Reused VCO-Buffer and a Type-I FLL with Rapid Phase Alignment

H. Li[1], T. Xu[1], X. Meng[1], J. Yin[1], R. P. Martins[1,2], P-I. Mak[1]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Conclusion 11:45 AM

Industry Invited

Session Chair: **Alicia Klinefelter,** NVIDIA, Durham, NC
Session Co-Chair: **Vivek De,** *Intel, Beaverton, OR*

8:00 AM

11.1 AMD MI300 Modular Chiplet Platform – HPC and AI Accelerator for Exa-Class Systems

A. Smith[1], E. Chapman[1], C. Patel[1], R. Swaminathan[1], J. Wuu[2], T. Huang[3], W. Jung[3], A. Kaganov[3], H. McIntyre[4], R. Mangaser[5]
[1]AMD, Austin, TX
[2]AMD, Fort Collins, CO
[3]AMD, Markham, Canada
[4]AMD, Santa Clara, CA
[5]AMD, Boxborough, MA

8:25 AM

11.2 A 3D Integrated Prototype System-on-Chip for Augmented Reality Applications Using Face-to-Face Wafer-Bonded 7nm Logic at <10μm Pitch with up to 40% Energy Reduction at Iso-Area Footprint

T. Wu, H. Liu, H. E. Sumbul, L. Yang, D. Baheti, J. Coriell, W. Koven, A. Krishnan, M. Mittal, M. T. Moreira, M. Waugaman, L. Ye, E. Beigne
Meta, Sunnyvale, CA

8:50 AM

11.3 Metis AIPU: A 12nm 15TOPS/W 209.6TOPS SoC for Cost- and Energy- `DS1` **Efficient Inference at the Edge**

P. A. Hager, B. Moons, S. Cosemans, I. A. Papistas, B. Rooseleer, J. Van Loon, R. Uytterhoeven, F. Zaruba, S. Koumousi, M. Stanisavljevic, S. Mach, S. Mutsaards, R. Khaddam Aljameh, G. H. Khov, B. Machiels, C. Olar, A. Psarras, S. Geursen, J. Vermeeren, Y. Lu, A. Maringanti, D. Ameta, L. Katselas, N. Hütter, M. Schmuck, S. Sivadas, K. Sharma, M. Oliveira, R. Aerne, N. Sharma, T. Soni, B. Bussolino, D. Pesut, M. Pallaro, A. Podlesnii, A. Lyrakis, Y. Ruffiner, M. Dazzi, J. Thiele, K. Goetschalckx, N. Bruschi, J. Doevenspeck, B. Verhoef, S. Linz, G. Garcea, J. Ferguson, I. Koltsidas, E. Eleftheriou
Axelera AI, Eindhoven, The Netherlands

9:15 AM

11.4 IBM NorthPole: An Architecture for Neural Network Inference with a 12nm `DS1` **Chip**

A. S. Cassidy[1], J. V. Arthur[2], F. Akopyan[3], A. Andreopoulos[2], R. Appuswamy[2], P. Datta[2], M. V. Debole[2], S. K. Esser[2], C. Ortega Otero[2], J. Sawada[1], B. Taba[2], A. Amir[2], D. Bablani[2], P. J. Carlson[2], M. D. Flickner[2], R. Gandhasri[2], G. J. Garreau[2], M. Ito[4], J. L. Klamo[2], J. A. Kusnitz[2], N. J. McClatchey[1], J. L. McKinstry[2], Y. Nakamura[4], T. K. Nayak[2], W. P. Risk[2], K. Schleupen[3], B. Shaw[2], J. Sivagnaname[1], D. F. Smith[2], I. Terrizzano[2], T. Ueda[4], D. Modha[2]
[1]IBM Research, Austin, TX
[2]IBM Research, San Jose, CA
[3]IBM Research, Yorktown, NY
[4]IBM Research, Tokyo, Japan

Break 9:40 AM

Electromagnetic Interface ICs for Information and Power

Session Chair: **Alyosha Molnar,** *Cornell University, Ithaca, NY*
Session Co-Chair: **Noriyuki Miura,** *Osaka University, Suita, Japan*

10:05 AM

12.1 Monolithically Integrated Sub-63fJ/b 8-Channel 256Gb/s Optical Transmitter with Autonomous Wavelength Locking in 45nm CMOS SOI
K. Omirzakhov, F. Aflatouni
University of Pennsylvania, Philadelphia, PA

10:30 AM

12.2 A mm-Wave/Sub-THz Synthesizer-Free Coherent Receiver with Phase Reconstruction Through Mixed-Signal Kramer-Kronig Processing
S. Ghozzy*, M. Allam*, E. A. Karahan, Z. Liu, K. Sengupta
Princeton University, Princeton, NJ
*Equally Credited Authors (ECAs)

10:55 AM

12.3 A Scalable and Instantaneously Wideband 5GS/s RF Correlator Based on
DS1 **Charge Thresholding Achieving 8-bit ENOB and 152 TOPS/W Compute Efficiency**
K. Rashed[1], A. Undavalli[2], S. Chakrabartty[2], A. Nagulu[2], A. Natarajan[1]
[1]Oregon State University, Corvallis, OR
[2]Washington University in St. Louis, St. Louis, MO

11:20 AM

12.4 A 19μW 200Mb/s IoT Tag Demonstrating High-Definition Video Streaming via a Digital-Switch-Based Reconfigurable 16-QAM Backscatter Communication Technique
Y. Zhang, R. Luo, J. Xiong, S. Liang, M. Meng
Tongji University, Shanghai, China

11:35 AM

12.5 A Packageless Anti-Tampering Tag Utilizing Unclonable Sub-THz Wave Scattering at the Chip-Item Interface
E. Lee, X. Chen, M. Ashok, J. Won, A. Chandrakasan, R. Han
Massachusetts Institute of Technology, Cambridge, MA

11:50 AM

12.6 A 64.4% Efficiency 5.8GHz RF Wireless Power Transfer Receiver with GaAs E-pHEMT Rectifier and 45.2μs MPPT Time SIDITO Buck-Boost Converter Using V_{oc} Prediction Scheme
K. Ichikawa[1], T. Iwata[1], S. Onishi[1], T. Higuchi[1], Y. Hirose[2], N. Sakai[2], K. Itoh[2], K. Miyaji[1]
[1]Shinshu University, Nagano, Japan
[2]Kanazawa Institute of Technology, Nonoichi, Japan

Conclusion 12:05 PM

High-Density Memory and Interfaces

Session Chair: Dong-Kyun Kim, *SK hynix, Icheon-si, Korea*
Session Co-Chair: Hidehiro Shiga, *KIOXIA, Yokohama, Japan*

8:00 AM

13.1 A 35.4Gb/s/pin 16Gb GDDR7 with a Low-Power Clocking Architecture and PAM3 IO Circuitry
J. Yang*, H. Ko*, K. Kim, H. Park, J. Park, J-H. Kang, J. Cha, S. Kim, Y. Kim, M. Park, G. Lee, K. Lee, S. Lee, G. Jeon, S. Jeong, Y. Joo, J. Cha, S. Hwang, B. Kim, S. Byeon, S. Lee, H. Park, J. Cho, J. Kim, SK hynix Semiconductor, Icheon, Korea; *Equally Credited Authors (ECAs)

8:25 AM

13.2 A 32Gb 8.0Gb/s/pin DDR5 SDRAM with a Symmetric-Mosaic Architecture in a 5th-Generation 10nm DRAM Process
I. Choi, S. Hong, K. Kim, J-S. Hwang, S. Woo, Y-S. Kim, C-R. Cho, E-Y. Lee, H-J. Lee, M-S. Jung, H-Y. Jung, J-S. Hwang, J-S. Yoon, W-M. Lim, H-J. Yoo, W-K. Lee, J-K. Oh, D-S. Lee, J-E. Lee, J-H. Kim, Y-K. Kim, S-J. Park, B-K. Ho, B-W. Na, H-I. Choi, C-K. Lee, S-J. Lee, H. Shin, Y-K. Lee, J-W. Ryu, S. Shin, S. Park, D. Lim, S-J. Bae, Y-S. Sohn, T-Y. Oh, S. Hwang Samsung Electronics, Hwaseong, Korea

8:50 AM

13.3 A 280-Layer 1Tb 4b/cell 3D-NAND Flash Memory with a 28.5Gb/mm² Areal Density and a 3.2GB/s High-Speed IO Rate
H. Kim, W. Jung, D-B. Kim, T-H. Kim, N. Lee, D. Shin, M. Kim, Y. Rho, H-J. Lee, Y. Hyun, J. Park, T. Kim, H. Kim, G. Lee, J. Lee, J. Jang, J. Park, S. Kim, S. C. Jeon, S. Kim, J-H. Song, M-S. Kim, T. Lee, B-K. Chun, T. Kim, Y. G. Lee, H. Lee, S. Lee, H. Lee, D. Cho, S-W. Nam, Y. Kim, K. Yoon, Y. Lee, S. Kim, J. Hwang, R. Song, H. Jang, J. Son, H. Jeon, M. Lee, M. Lee, K. Kim, E. Lee, M. Lee, S. Jo, C. H. Kim, J. C. Park, K. Yun, S. Seol, J-H. Cho, S. Lee, J-Y. Lee, S-H. Hur Samsung Electronics, Hwaseong, Korea

9:15 AM

13.4 A 48GB 16-High 1280GB/s HBM3E DRAM with All-Around Power TSV and a 6-Phase RDQS Scheme for TSV Area Optimization
J. Lee*, K. Cho*, C. K. Lee, Y. Lee, J-H. Park, S-H. Oh, Y. Ju, C. Jeong, H. S. Cho, J. Lee, T-S. Yun, J. H. Cho, S. Oh, J. Moon, Y-J. Park, H-S. Choi, I-K. Kim, S. M. Yang, S-Y. Kim, J. Jang, J. Kim, S-H. Lee, Y. Jeon, J. Park, T-K. Kim, D. Ka, S. Oh, J. Kim, J. Jeon, S. Kim, K. T. Kim, T. Kim, H. Yang, D. Yang, M. Lee, H. Song, D. Jang, J. Shin, H. Kim, C. Baek, H. Jeong, J. Yoon, S-K. Lim, K. Y. Lee, Y. J. Koo, M-J. Park, J. Cho, J. Kim SK hynix Semiconductor, Icheon, Korea; *Equally Credited Authors (ECAs)

Break 9:40 AM
10:05 AM

DS1
13.5 A 64Gb/s/pin PAM4 Single-Ended Transmitter with a Merged Pre-Emphasis Capacitive-Peaking Crosstalk Cancellation Scheme for Memory Interfaces in 28nm CMOS
W. Wu*, H. Wu*, L. Zhong, X. Cheng, X. Luo, D. Xu, C. Wang, Z. Li, Q. Pan Southern University of Science and Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

10:30 AM

13.6 A 16Gb 37Gb/s GDDR7 DRAM with PAM3-Optimized TRX Equalization and ZQ Calibration
S-Y. Cho, M-C. Choi, J. Baek, D. An, S. Kim, D. Lee, S. Yang, G-Y. Kang, J. Park, K. Lee, H-C. Jung, G. Cho, C. Lee, H-R. Kim, Y-J. Shin, H. Park, S. Lee, J. Kim, B. Won, J. Mok, K. Kim, U. Lim, H-J. Jin, Y. Lee, Y-T. Kim, H. Ha, J. Ahn, W. Sung, Y. Jang, H. Song, H. Ban, T. Park, T-Y. Oh, C. Yoo, S. Hwang, Samsung Electronics, Hwasung, Korea

10:55 AM

13.7 A 1Tb Density 3b/Cell 3D-NAND Flash on a 2YY Tier Technology with a 300MB/s Write Throughput
K. Kawai[1], Y. Einaga[1], Y. Oikawa[1], Y. He[2], B. Iorio[3], S. Yamada[1], Y. Kamata[1], T. Iwasaki[2], A. D'alessandro[3], E. Yu[2], A. Muralidharan[4], Q. Li[2], H. Nguyen[2], K-F. Chan[2], M. Piccardi[2], T. Ichikawa[1], J. Yu[2], G. Wang[2], K. Kim[2], C. Kim[2], P. Mangalindan[4], H. Yun[2], L. Nubile[3], K. Verma[2], S. Bhushan[2], D. Srinivasan[2], H. Kuge[1], R. Subramanian[5], J. Kishimoto[1], T. Kamijo[1], P. Musunuri[2], C. Siau[2], R. Ghodsi[2], [1]Micron Technology, Tokyo, Japan; [2]Micron Technology, San Jose, CA [3]Micron Technology, Avezzano, Italy; [4]Micron Technology, Folsom, CA [5]Micron Technology, Hyderabad, India

11:20 AM

13.8 A 1a-nm 1.05V 10.5Gb/s/pin 16Gb LPDDR5 Turbo DRAM with a WCK-Correction Strategy, a Voltage-Offset-Calibrated Receiver and Parasitic Capacitance Reduction
Y. Seo*, J. Choi*, S. Cho, H. Han, W. Kim, G. Ryu, J. Ahn, Y. Cho, S. Choi, S. Lee, W. Lee, C. Lee, K. Kim, S. Lee, S. Park, M. Choi, S. Lee, M. Kim, T. Shin, H. Jeong, H. Kim, H. Song, Y. Hong, S. Yoon, G. Park, H. You, C. Choi, H-K. Jung, J. Cho, J. Kim SK hynix, Icheon, Korea; *Equally Credited Authors (ECAs)

11:35 AM

13.9 A 25.2Gb/s/pin NRZ/PAM-3 Dual-Mode Transmitter with Embedded Partial DBI Achieving a 133% I/O Bandwidth/Pin Efficiency and a 19.3% DBI Efficiency
C. Han*, K-S. Lee*, J-H. Chae Kwangwoon University, Seoul, Korea; *Equally Credited Authors (ECAs)

11:50 AM

13.10 A 4nm 48Gb/s/wire Single-Ended NRZ Parallel Transceiver with Offset-Calibration and Equalization Schemes For Next-Generation Memory Interfaces and Chiplets
K. Seong, W. Oh, H. Lee, G. Bae, Y. Suh, H. Lee, J. Kim, E. Kim, Y. Kang, G. Mo, Y. Lee, M. Kim, S. Lee, D. Park, B-J. Yoo, H-G. Rhew, J. Shin, Samsung Electronics, Hwaseong, Korea

Conclusion 12:05 PM

Digital Techniques for System Adaptation, Power Management and Clocking

Session Chair: Yvain Thonnart, *CEA-List, Grenoble, France*
Session Co-Chair: Heein Yoon, *Ulsan National Institute of Science and Technology, Ulsan, Korea*

1:30 PM

14.1   A Software-Assisted Peak Current Regulation Scheme to Improve Power-Limited Inference Performance in a 5nm AI SoC

M. Kar[1], J. Silberman[1], S. Venkataramani[1], V. Srinivasan[1], B. Fleischer[1], J. Rubin[1], J. Lancaster[1], S. K. Lee[1], M. Cohen[1], M. Ziegler[1], N. Cao[1], S. Woodward[2], A. Agrawal[1], C. Zhou[1], P. Chatarasi[1], T. Gooding[2], M. Guillorn[1], B. Hekmatshoartabari[1], P. Jacob[1], R. Jain[1], S. Jain[1], J. Jung[1], K. H. Kim[1], S. Koswatta[1], M. Lutz[1], A. Mannari[3], A. Mathew[4], I. Nair[1], A. Ranjan[1], Z. Ren[1], S. Rider[5], T. Rower[1], D. Satterfield[6], M. Schaal[1], S. Sen[1], G. Tellez[1], H. Tran[1], W. Wang[1], V. Zalani[1], J. Zhang[1], X. Zhang[1], V. Shah[7], R. Senger[1], A. Kumar[1], P-F. Lu[1], L. Chang[1]
[1]IBM Research, Yorktown Heights, NY; [2]IBM, Rochester, MN; [3]IBM Research, Zurich, Switzerland [4]IBM, Austin, TX; [5]IBM, Poughkeepsie, NY; [6]IBM Research, Lowell, MA [7]IBM, Hursley, United Kingdom

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14.2 `DS1`   Proactive Voltage Droop Mitigation Using Dual-Proportional-Derivative Control Based on Current and Voltage Prediction Applied to a Multicore Processor in 28nm CMOS

W. Shan, K. Zhou, K. Li, Y. Du, Z. Chen, J. Qian, H. Ge, J. Yang, X. Si
Southeast University, Nanjing, China

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14.3   A 3nm Adaptive Clock Duty-Cycle Controller for Mitigating Aging-Induced Clock Duty-Cycle Distortion

D. Yingling[1], Y. Peng[1], R. Vachon[1], D. Pal[1], S. Jariwala[2], F. Cabral[3], J. Hu[2], R. Verma[2], V. Chiranji[2], A. Kumar[2], S. Sarma[2], K. Bowman[1]
[1]Qualcomm, Raleigh, NC; [2]Qualcomm, San Diego, CA; [3]Qualcomm, Cork, Ireland

2:45 PM

14.4   A Fully Digital Current Sensor Offering Per-Core Runtime Power for System Budgeting in a 4nm-Plus Octa-Core CPU

*C-Y. Lu[1], B-J. Huang[1], M-C. Chen[1], O. Tsai[1], A. Tsai[1], E-W. Fang[1], Y. Cho[1], H. H. Chen[1], P. Kao[1], E. Wang[1], H. Mair[2], S-A. Hwang[1], *[1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, Austin, TX

3:00 PM

14.5 `DS1`   A 12nm Linux-SMP-Capable RISC-V SoC with 14 Accelerator Types, Distributed Hardware Power Management and Flexible NoC-Based Data Orchestration

M. Cassel dos Santos[1], T. Jia*[2], J. Zuckerman*[1], M. Cochet*[3], D. Giri[1], E. J. Loscalzo[1], K. Swaminathan[3], T. Tambe[2], J. J. Zhang[2], A. Buyuktosunoglu[3], K-L. Chiu[1], G. Di Guglielmo[1], P. Mantovani[1], L. Piccolboni[1], G. Tombesi[3], D. Trilla[3], J-D. Wellman[3], E-Y. Yang[2], A. Amarnath[3], Y. Jing[4], B. Mishra[4], J. Park[2], V. Suresh[4], S. Adve[4], P. Bose[3], D. Brooks[2], L. P. Carloni[1], K. L. Shepard[1], G-Y. Wei[2], *[1]Columbia University, New York, NY
[2]Harvard University, Cambridge, MA; [3]IBM Research, Yorktown Heights, NY [4]University of Illinois, Urbana, IL; *Equally Credited Authors (ECAs)

Break 3:15 PM
3:35 PM

14.6   A 10A Computational Digital LDO Achieving 263A/mm² Current Density with Distributed Power-Gating Switches and Time-Based Fast-Transient Controller for Mobile SoC Application in 3nm GAAFET

D. Lee, S. Kim, T. Nomiyama, D-H. Jung, D. Kim, J. Lee, S. Kwak
Samsung Electronics, Hwaseong, Korea

4:00 PM

14.7   A 0.45V 0.72mW 2.4GHz Bias-Current-Free Fractional-N Hybrid PLL Using a Voltage-Mode Phase Interpolator in 28nm CMOS

L. Feng, X. Ji, L. Kuang, Q. Liao, S. Han, J. Zhao, W. Rhee, Z. Wang
Tsinghua University, Beijing, China

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14.8   KASP: A 96.8% 10-Keyword Accuracy and 1.68μJ/Classification Keyword Spotting and Speaker Verification Processor Using Adaptive Beamforming and Progressive Wake-Up

J. Xiao[1], X. Zhang[1], S. Zhu[1], Z. Yang[1], M. Du[1], C. Ji[1], Y. Long[1], X. Chen[2], X. Miao[2], L. Zhou[1], L. Chang[1], S. Liu[1], J. Zhou[1]
[1]University of Electronic Science and Technology of China, Chengdu, China
[2]China Micro Semicon, Chengdu, China

4:50 PM

14.9   A Monolithic 10.5W/mm² 600MHz Top-Metal and C4 Planar Spiral Inductor-Based Integrated Buck Voltage Regulator on 16nm-Class CMOS

S. Kim, H. K. Krishnamurthy, Z. Ahmed, N. Desai, S. Weng, A. Augustine, H. T. Do, J. Yu, P. D. Bach, X. Liu, K. Radhakrishnan, K. Ravichandran, J. W. Tschanz, V. De
Intel, Hillsboro, OR

5:05 PM

14.10   34.7A/mm² Scalable Distributed All-Digital 6×6 Dot-LDOs Featuring Freely Linkable Current-Sharing Network: A Fine-Grained On-Chip Power Delivery Solution in 28nm CMOS

Y-J. Lee[1,2], W. Jang[1,2], H-H. Bae[1], J-H. Cho[1], H-S. Kim[1]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

Conclusion 5:20 PM

Embedded Memories & Ising Computing

Session Chair: **Takashi Ito**, *Renesas, Kodaira-shi, Tokyo, Japan*
Session Co-Chair: **John Wuu**, *Advanced Micro Devices, Fort Collins, CO*

1:30 PM

15.1 A 0.795fJ/b Physically-Unclonable-Function-Protected TCAM for a
DS1 **Software-Defined Networking Switch**

Z. Yue[1], X. Xiang[1], F. Tu[2], Y. Wang[1], Y. Wang[1], S. Wei[1], Y. Hu[1], S. Yin[1]
[1]Tsinghua University, Beijing, China
[2]Hong Kong University of Science and Technology, Hong Kong, China

1:55 PM

15.2 A 2048×60m4 SRAM Design in Intel 4 with Around-the-Array Power-Delivery Scheme Using PowerVia

D. Kim, Y. Kim, A. Shrivastava, G. Park, A. Mahadevan Pillai, K. Bannore, T. Doan, M. Rahman, G. Baek, C. Ong, X. Wang, Z. Guo, E. Karl
Intel, Hillsboro, OR

2:20 PM

15.3 A 3nm FinFET 4.3GHz 21.1Mb/mm² Double-Pumping 1-Read and 1-Write Pseudo-2-Port SRAM with Folded-Bitline Multi-Bank Architecture

M. Haraguchi[1], Y. Fujino[1], Y. Yokoyama[1], M-H. Chang[2], Y-H. Hsu[2], H-C. Cheng[2], K. Nii[1], Y. Wang[2], T-Y. J. Chang[2]
[1]TSMC Design Technology Japan, Yokohama, Japan
[2]TSMC, Hsinchu, Taiwan

2:45 PM

15.4 Self-Enabled Write-Assist Cells for High-Density SRAM in a Resistance-Dominated Technology Node

M. Yeo[1], K. Cho[1], G. Kim[1], W. J. Jo[1], J. Oh[1], S. Kim[1], K. Baek[1], S. Park[1], S. J. Yei[1], S-O. Jung[1,2]
[1]Yonsei University, Seoul, Korea
[2]Articron, Ansan, Korea

3:00 PM

15.5 LISA: A 576×4 All-in-One Replica-Spin Continuous-Time Latch-Based Ising Computer Using Massively-Parallel Random-Number Generations and Replica Equalizations

*J. Bae *[1], J. Koo *[2], C. Shim *[1], B. Kim[1]*
[1]University of California, Santa Barbara, CA
[2]Sejong University, Seoul, Korea
*Equally Credited Authors (ECAs)

Break 3:15 PM
3:35 PM

15.6 e-Chimera: A Scalable SRAM-Based Ising Macro with an Enhanced-Chimera Topology for Solving Combinatorial-Optimization Problems Within Memory

J. Bae, C. Shim, B. Kim, University of California, Santa Barbara, CA

4:00 PM

15.7 A 32Mb RRAM in a 12nm FinFet Technology with a 0.0249μm² Bitcell, a 3.2GB/S Read Throughput, a 10kCycle Write Endurance and 10-Year Retention at 105°C

Y-C. Huang, S-H. Liu, H-S. Chen, H-C. Feng, C-F. Li, C-Y. Yang, W-K. Chang, C-F. Yang, C-Y. Wu, Y-C. Lin, T-T. Yang, C-Y. Chang, W-T. Chu, H. Chuang, Y. Wang, Y-D. Chih, T-Y. J. Chang
TSMC, Hsinchu, Taiwan

4:25 PM

15.8 A 22nm 10.8Mb Embedded STT-MRAM Macro Achieving over 200MHz Random-Read Access and a 10.4MB/s Write Throughput with an In-Field Programmable 0.3Mb MTJ-OTP for High-End MCUs

T. Ogawa, K. Matsubara, Y. Taito, T. Saito, M. Izuna, K. Takeda, Y. Kaneda, T. Shimoi, H. Mitani, T. Ito, T. Kono
Renesas Electronics, Tokyo, Japan

4:50 PM

15.9 A 16nm 16Mb Embedded STT-MRAM with 20ns Write Time, a 10¹² Write Endurance and Integrated Margin-Expansion Schemes

K-F. Lin, H. Noguchi*, Y-C. Shih, P-F. Yuh, Y-J. Lee, T-C. Chang, S-P. Huang, Y-F. Lin, C-Y. Lee, Y-H. Huang, J-C. Tsai, S. Adham, P. Noel, R. Yazdi, M. Gershoig, Y. Shin, V. Joshi, T. Wong, M-R. Jiang, J. J. Wu, C-T. Cheng, Y-J. Wang, H. Chuang, Y-D. Chih, Y. Wang, T-Y. J. Chang*
TSMC, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

Conclusion 5:15 PM

Security: From Processors to Circuits

Session Chair: **Sanu Mathew,** Intel, Portland, OR
Session Co-Chair: **Takeshi Sugawara,**
                   The University of Electro-Communications, Tokyo, Japan

1:30 PM

16.1 A 2.7-to-13.3µJ/boot/slot Flexible RNS-CKKS Processor in 28nm CMOS Technology for FHE-Based Privacy-Preserving Computing
H. Lee*, H. Kwon*, Y. Lee
Pohang University of Science and Technology, Pohang, Korea
*Equally Credited Authors (ECAs)

1:55 PM

16.2 A 28nm 69.4kOPS 4.4µJ/Op Versatile Post-Quantum Crypto-Processor
DS1 Across Multiple Mathematical Problems
Y. Zhu[1], W. Zhu[1,2], Y. Ouyang[1], J. Sun[1,2], M. Zhu[3], Q. Zhao[1,2], J. Yang[1], C. Chen[1,2], Q. Tao[1,2], G. Yang[1,2], A. Zhang[1], S. Wei[1,2], L. Liu[1,2]
[1]Tsinghua University, Beijing, China
[2]Beijing National Research Center for Information Science and Technology(BNRist), Beijing, China
[3]Micro Innovation Integrated Circuit Design Co.,Ltd, Wuxi, China

2:20 PM

16.3 3nm Physical Unclonable Function with Multi-Mode Self-Destruction and 3.48×10^{-5} Bit Error Rate
E. Hunt-Schroeder[1], P. Lin-Butler[2], A. Degada[1], T. Xia[2]
[1]Marvell, Burlington, VT
[2]University of Vermont, Burlington, VT

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16.4 High-Density and Low-Power PUF Designs in 5nm Achieving 23× and 39× BER Reduction After Unstable Bit Detection and Masking
S. S. Kudva[1], M. E. Sinangil[1], S. Tell[2], N. Nedovic[1], S. Song[1], B. Zimmer[1], C. T. Gray[2]
[1]Nvidia, Santa Clara, CA
[2]Nvidia, Durham, NC

Break 3:10 PM
3:35 PM

16.5 A Synthesizable Design-Agnostic Timing Fault Injection Monitor Covering
DS1 2MHz to 1.26GHz Clocks in 65nm CMOS
Y. He, K. Yang
Rice University, Houston, TX

4:00 PM

16.6 PACTOR: A Variation-Tolerant Probing-Attack Detector for a 2.5Gb/s×4-
DS1 Channel Chip-to-Chip Interface in 28nm CMOS
M. Li[1], Z. Wang[1], S. K. Mathew[2], V. De[2], M. Seok[1]
[1]Columbia University, New York, NY
[2]Intel, Hillsboro, OR

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16.7 Power and EM Side-Channel-Attack-Resilient AES-128 Core with Round-
DS1 Aligned Globally-Synchronous-Locally-Asynchronous Operation Based
on Tunable Replica Circuits
S. Oruganti*[1], M. Wang*[1], V. V. Iyer[1], Y. Wang[1], M. Yang[1], R. Kumar[2], S. K. Mathew[2], J. P. Kulkarni[1]
[1]University of Texas, Austin, TX
[2]Intel, Hillsboro, OR
*Equally Credited Authors (ECAs)

4:50 PM

16.8 A 60Mb/s TRNG with PVT-Variation-Tolerant Design Based on STR in 4nm
J. Park, Y-K. Lee, K. Bohdan, Y. Choi, J. Shin, H-G. Rhew, J. Shin
Samsung Electronics, Hwaseong, Korea

Conclusion 5:15 PM

Emerging Sensing and Computing Technologies

Session Chair: **Rabia Yazicigil,** *Boston University, Boston, MA*
Session Co-Chair: **Denis Daly,** *Apple, Wellesley, MA*

1:30 PM

17.1 **Omnidirectional Magnetoelectric Power Transfer for Miniaturized**
DS2 **Biomedical Implants via Active Echo**
W. Wang, Z. Yu, Y. Zou, J. Woods, P. Chari, J. T. Robinson, K. Yang
Rice University, Houston, TX

1:55 PM

17.2 **A Miniature Multi-Nuclei NMR/MRI Platform with a High-Voltage SOI**
ASIC Achieving a 134.4dB Image SNR with a $173\times250\times103\mu m^3$
Resolution
S. Fan[1], Q. Zhou[1], K. M. LEI[1], R. P. Martins[1,2], P-I. Mak[1]
[1]University of Macau, Macau, China
[2]Instituto Superior Técnico/Universidade de Lisboa, Lisbon, Portugal"

2:20 PM

17.3 **A Fully Wireless, Miniaturized, Multicolor Fluorescence Image Sensor**
DS2 **Implant for Real-Time Monitoring in Cancer Therapy**
*R. Rabbani *[1], M. Roschelle *[1], S. Gweon[1], R. Kumar[1], A. Vercruysse[1], N. W. Cho[2],*
M. H. Spitzer[2], A. M. Niknejad[1], V. M. Stojanovic[1], M. Anwar[1,2]
[1]University of California, Berkeley, CA; [2]University of California, San Francisco, CA
*Equally Credited Authors (ECAs)

2:45 PM

17.4 **Environmentally Friendly Disposable Circuit and Battery System for**
DS2 **Reducing Impact of E-Wastes**
*N. Miura *[1], H. Taguchi *[1], K. Watanabe[2], M. Nohara[1], T. Makita[3], M. Tanabe[3],*
T. Wakimoto[3], S. Kumagai[2], H. Nosaka[1], A. Aratake[1], T. Okamoto[2], S. Watanabe[2],
J. Takeya[2], T. Komatsu[1], [1]Nippon Telegraph and Telephone, Atugi, Japan
[2]University of Tokyo, Kashiwa, Japan; [3]PI-CRYSTAL Incorporation, Kashiwa, Japan
*Equally Credited Authors (ECAs)

3:00 PM

17.5 **A 24V Mini-Coil Magnetic Neural Stimulator with Closed-Loop Deadtime**
Control and ZCS Control Achieving 99.76% Charge Recovery Efficiency
*Y. Fan *, Y. Liu *, G. Topalli, R. Lycke, L. Luan, C. Xie, T. Chi*
Rice University, Houston, TX; *Equally Credited Authors (ECAs)

Break 3:15 PM
3:35 PM

17.6 **Fully Integrated CMOS Ferrofluidic Biomolecular Processing Platform**
with On-Chip Droplet-Based Manipulation, Multiplexing and Sensing
*D. Lee *[1], K-S. Choi *[1], F. Jiang *[1], H. Liu[1], D. Jung[2], Y. Kong[1], M. Saif[1], Z. Huang[1],*
J. Wang[1], H. Wang[1], [1]ETH Zürich, Zurich, Switzerland; [2]Qualcomm, Santa Clara, CA
*Equally Credited Authors (ECAs)

4:00 PM

17.7 **Droplet Microfluidics Co-Designed with Real-Time CMOS Luminescence**
DS2 **Sensing and Impedance Spectroscopy of 4nL Droplets at a 67mm/s**
Velocity
Q. Liu, D. Arguijo Mendoza, A. Yasar, D. Caygara, A. Kassem, D. Densmore,
R. T. Yazicigil, Boston University, Boston, MA

4:25 PM

17.8 **0.4V 988nW Time-Domain Audio Feature Extraction for Keyword Spotting**
Using Injection-Locked Oscillators
A. Mostafa, E. Hardy, F. Badets, CEA-Léti, Grenoble, France

4:50 PM

17.9 **A 1.8% FAR, 2ms Decision Latency, 1.73nJ/Decision Keywords Spotting**
(KWS) Chip Incorporating Transfer-Computing Speaker Verification,
Hybrid-Domain Computing and Scalable 5T-SRAM
F. Tan[1], W-H. Yu[1], J. Lin[1], K-F. Un[1], R. P. Martins[1,2], P-I. Mak[1]
[1]University of Macau, Macau, China; [2]University of Lisboa, Lisboa, Portugal

5:05 PM

17.10 A 0.4V, 750nW, Individually Accessible Wireless Capacitive Sensor
Interface IC for a Tactile Sensing Network
H. Hao, A. G. Richardson, Y. Ding, L. Du, M. G. Allen, J. Van der Spiegel, F. Aflatouni
University of Pennsylvania, Philadelphia, PA

5:20 PM

17.11 A 9mW Ultrasonic Through Transmission Transceiver for Non-Invasive
Intracranial Pressure Sensing
G. Topalli[1], Y. Fan[1], M. Y. Cheung[1], A. Veeraraghavan[1], M. Hirzallah[2], T. Chi[1]
[1]Rice University, Houston, TX; [2]Baylor Collage of Medicine, Houston, TX

Conclusion 5:35 PM

High-Performance Optical Transceivers

Session Chair: **Tamer Ali,** *Mediatek, Laguna Hills, CA*
Session Co-Chair: **Hyo Gyuem Rhew,** *Samsung, Hwaseong-si, Gyeonggi-do, Korea*

1:30 PM

18.1 A 600Gb/s DP-QAM64 Coherent Optical Transceiver Front-End with 4x105GS/s 8b ADC/DAC in 16nm CMOS

G. Li[1], A. Garg[1], T. He[1], U. Singh[1], J. Zhang[1], L. Rao[1], C. Liu[1], M. Nazari[1], Y. Liu[1], Y. Liu[1], H. Zhang[1], T. Ali[1,2], H-G. Rhew[1,3], J. Ru[1,4], D. Cui[1], A. Nazemi[1], B. Zhang[1], A. Momtaz[1], J. Cao[1]
[1]Broadcom, Irvine, CA
[2]MediaTek, Irvine, CA
[3]Samsung Electronics, Hwaseong, Korea
[4]Peking University, Beijing, China

1:55 PM

18.2 A 4×64Gb/s NRZ 1.3pJ/b Co-Packaged and Fiber-Terminated 4-Ch
DS1 VCSEL-Based Optical Transmitter

S. Mondal, J. Qiu, S. Krishnamurthy, J. Kennedy, S. Bose, T. Acikalin, S. Yamada, J. Jaussi, M. Mansuri
Intel, Hillsboro, OR

2:20 PM

18.3 An 8b 160GS/s 57GHz Bandwidth Time-Interleaved DAC and Driver-Based Transmitter with Adaptive Calibration for 800Gb/s Coherent Optical Applications in 5nm

F. Ahmad[1], A. Mellati[1], A. Fernandez[2], A. Iyer[3], A. Fan[1], B. Reyes[2], C. Abidin [1], C. Nani[4], D. Albano[4], F. Solis[2], G. Minoia[4], G. Hatcher[1], H. Carrer[2], K. Kota[1], L. Wang[1], M. Bachu[3], M. Garampazzi[4], M. Hassanpourghadi[1], N. Fan[1], P. Prabha[1], R. Nguyen[1], S. Ho[5], T. Dusatko[5], T. Wu[1], W. Elsharkasy[1], Z. Sun[6], S. Jantzi[1], L. Tse[3]
[1]Marvell, Irvine, CA
[2]Marvell, Cordoba, Argentina
[3]Marvell, Santa Clara, CA
[4]Marvell, Pavia, Italy
[5]Marvell, Vancouver, Canada
[6]Marvell, Singapore, Singapore

2:45 PM

18.4 A 200GS/s 8b 20fJ/c-s Receiver with >60GHz AFE Bandwidth for 800Gb/s Optical Coherent Communications in 5nm FinFET

R. L. Nguyen[1], A. Mellati[1], A. Fernandez[2], A. Iyer[3], A. Fan[1], B. Reyes[2], C. Abidin[1], C. Nani[4], D. Albano[4], F. Ahmad[1], F. Solis[2], G. Minoia[4], G. Hatcher[1], M. Bachu[3], M. Garampazzi[4], M. Hassanpourghadi[1], N. Fan[1], P. Prabha[1], S. Fan[3], S. Ho[5], T. Dusatko[5], T. Wu[1], W. Elsharkasy[1], Z. Sun[6], S. Jantzi[1], L. Tse[3]
[1]Marvell, Irvine, CA
[2]Marvell, Cordoba, Argentina
[3]Marvell, Santa Clara, CA
[4]Marvell, Pavia, Italy
[5]Marvell, Vancouver, Canada
[6]Marvell, Singapore, Singapore

Break 3:10 PM

RF to mm-Wave Oscillators and Multipliers

Session Chair: **Hongtao Xu,** *Fudan University, Shanghai, China*
Session Co-Chair: **Swaminathan Sankaran,** *Texas Instruments, Allen, TX*

<div align="center">3:35 PM</div>

19.1 A 7.5GHz Subharmonic Injection-Locked Clock Multiplier with a 62.5MHz Reference, -259.7dB FoM$_J$, and -56.6dBc Reference Spur
H. Choi, S. Cho
Korea Advanced Institute of Science and Technology, Daejeon, Korea

<div align="center">4:00 PM</div>

19.2 A 12.4% Efficiency, 11dBm P$_{sat}$, Odd-Harmonics-Recycling, 62-to-92GHz CMOS Frequency Quadrupler Using an Amplitude-Phase Coordinating Technique
Z. Lin[1,2], Y. Shen[1,2], Y. Ding[1], S. Hu[1,2]
[1]Southeast University, Nanjing, China
[2]Purple Mountain Laboratories, Nanjing, China

<div align="center">4:25 PM</div>

19.3 An 8.9-to-21.9GHz Single-Core Oscillator with Reconfigurable Class-F^{-1} and Enhanced-Colpitts Dual-Mode Operation Achieving 209dBc/Hz FoM$_T$
Z. Kang, C. Yu, L. Wu
Chinese University of Hong Kong, Shenzhen, China

<div align="center">4:50 PM</div>

19.4 A 0.07mm^2 20-to-23.8GHz 8-phase Oscillator Incorporating Magnetic + Dual-Injection Coupling Achieving 189.2dBc/Hz FoM$_{@10MHz}$ and 200.7dBc/Hz FoM$_A$ in 65nm CMOS
*Y. Zhao *[1], C. Fan *[1], Q. Fang[1], G. Zhang[1], J. Yin[2], P-I. Mak[2], L. Geng[1]*
[1]Xi'an JiaoTong University, Xi'an, China
[2]University of Macau, Macao, China
*Equally Credited Authors (ECAs)

<div align="center">5:05 PM</div>

19.5 A 13.7-to-41.5GHz 214.1dBc/Hz FoM$_T$ Quad-Core Quad-Mode VCO Using an Oscillation-Mode-Splitting Technique
H. Ge, H. Jia, W. Deng, R. Ma, Z. Wang, B. Chi
Tsinghua University, Beijing, China

<div align="center">**Conclusion 5:20 PM**</div>

Demonstration Session 2, Tuesday, February 20th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 19th, and Tuesday February 20th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2024, as noted by the symbol **DS2**

17.1 Omnidirectional Magnetoelectric Power Transfer for Miniaturized Biomedical Implants via Active Echo

17.3 A Fully Wireless, Miniaturized, Multicolor Fluorescence Image Sensor Implant for Real-Time Monitoring in Cancer Therapy

17.4 Environmentally Friendly Disposable Circuit and Battery System for Reducing Impact of E-Wastes

17.7 Droplet Microfluidics Co-Designed with Real-Time CMOS Luminescence Sensing and Impedance Spectroscopy of 4nL Droplets at a 67mm/s Velocity

20.3 A 23.9TOPS/W @ 0.8V, 130TOPS AI Accelerator with 16× Performance-Accelerable Pruning in 14nm Heterogeneous Embedded MPU for Real-Time Robot Applications

20.5 C-Transformer: A 2.6-to-18.1μJ/Token Homogeneous DNN-Transformer/Spiking-Transformer Processor with Big-Little Network and Implicit Weight Generation for Large Language Models

20.6 LSPU: A Fully Integrated Real-Time LiDAR-SLAM SoC with Point-Neural-Network Segmentation and Multi-Level kNN Acceleration

20.7 NeuGPU: A 18.5mJ/Iter Neural-Graphics Processing Unit for Instant-Modeling and Real-Time Rendering with Segmented-Hashing Architecture

20.8 Space-Mate: A 303.5mW Real-Time Sparse Mixture-of-Experts-Based NeRF-SLAM Processor for Mobile Spatial Computing

23.2 A 1mm² Software-Defined Dual-Mode Bluetooth Transceiver with 10dBm Maximum TX Power and -98.2dBm Sensitivity 2.96mW RX Power at 1Mb/s

23.5 A 7.6mW IR-UWB Receiver Achieving −13dBm Blocker Resilience with a Linear RF Front-End

24.1 A 90-to-180GHz APD-Integrated Transmitter Achieving 18dBm P_{sat} in 28nm CMOS

26.5 A 977μW Capacitive Touch Sensor with Noise-Immune Excitation Source and Direct Lock-In ADC Achieving 25.2pJ/step Energy Efficiency

28.6 An 87% Efficient 2V-Input, 200A Voltage Regulator Chiplet Enabling Vertical Power Delivery in Multi-kW Systems-on-Package

29.5 A Portable 14GHz Dual-Mode Pulse and Continuous-Wave Electron Paramagnetic Resonance Spectrometer Using a Subharmonic Direct Conversion Receiver

30.1 A 40nm VLIW Edge Accelerator with 5MB of 0.256pJ/b RRAM and a Localization Solver for Bristle Robot Surveillance

30.6 Vecim: A 289.13GOPS/W RISC-V Vector Co-Processor with Compute-in-Memory Vector Register File for Efficient High-Performance Computing

31.5 A 750-mW, 37% Peak Efficiency Isolated DC-DC Converter with 54/18-Mb/s Full-Duplex Communication Using a Single Pair of Transformers

32.1 A 47GHz 4-Way Doherty PA with 23.7dBm P_{1dB} and 21.7% / 13.1% PAE at 6 / 12dB Back-Off Supporting 2000MHz 5G NR 64-QAM OFDM

32.5 E-band (71-to-86GHz) GaN Power Amplifier with 4.37W Output Power and 18.5% PAE for 5G Backhaul

33.1 A High-Accuracy and Energy-Efficient Zero-Shot-Retraining Seizure-Detection Processor with Hybrid-Feature-Driven Adaptive Processing and Learning-Based Adaptive Channel Selection

33.2 A Sub-1μJ/class Headset-Integrated Mind Imagery and Control SoC for VR/MR Applications with Teacher-Student CNN and General-Purpose Instruction Set Architecture

33.7 An Adhesive Interposer-Based Reconfigurable Multi-Sensor Patch Interface with On-Chip Application Tunable Time-Domain Feature Extraction

33.9 A Miniature Neural Interface Implant with a 95% Charging Efficiency Optical Stimulator and an 81.9dB SNDR ΔΣM-Based Recording Frontend

33.10 A 2.7ps-ToF-Resolution and 12.5mW Frequency-Domain NIRS Readout IC with Dynamic Light Sensing Frontend and Cross-Coupling-Free Inter-Stabilized Data Converter

34.6 A 28nm 72.12TFLOPS/W Hybrid-Domain Outer-Product Based Floating-Point SRAM Computing-in-Memory Macro with Logarithm Bit-Width Residual ADC

EE4:   Generative AI for Chip Design

Organizer:	**Johan Vanderhaegen,** G*oogle, Mountain View, CA*
Co-Organizer:	**Wu-Hsin Chen**, *Qualcomm, San Diego, CA*
	JuangYing Chue, *Etron, Taipei, Taiwan*
	Jae-sun Seo, *Cornell Tech, New York, NY*
	ShonHang Wen, *Mediatek, Hsinchu, Taiwan*
Moderator:	**Jan Rabaey**, *University of California, Berkeley, CA*
	and imec, Leuven, Belgium

With the emergence of machine learning and generative AI, many types of jobs are being transformed by GPT-based tools. Large Language Models are starting to be used for education and can be used to contribute to publications, and AI is being embedded into EDA tools. Join this evening panel with experts from industry and academia to discuss how generative AI or AI in general will change IC design.

Panelists:	**Thomas Andersen**, *Synopsys, Mountain View, CA*
	Edith Beigné, *Meta, Menlo Park, CA*
	Vidya Chhabria, *Arizona State University, Phoenix, AZ*
	Georges Gielen, *KU Leuven, Leuven, Belgium*
	Rajeev Jain, *Qualcomm, San Diego, CA*
	Hammond Pearce, *University of New South-Wales,*
	Sydney, Australia

EE5:   The Legacy of Gordon Moore

Organizer:	**Bodhisatwa Sadhu,** *IBM T. J. Watson Research Center,*
	Yorktown Heights, NY
Co-Organizers:	**Kaushik Sengupta**, *Princeton University, Princeton, NJ*
	Tanay Karnik, *Intel, Hillsboro, OR*
	Shahrzad Naraghi, *Legato Logic, San Jose, CA*
Moderator:	**Thomas Lee**, *Stanford University, Stanford, CA*

Moore's Law has propelled the semiconductor industry for decades, transforming the world through advancements in digital electronics, and to some extent, analog and RF electronics. These advancements have fueled other engineering fields such as artificial intelligence, biomedical engineering and quantum engineering. In this session, we will have a fireside chat with semiconductor and IC design luminaries celebrating the life and legacy of Gordon Moore, discussing the impact of Moore's law on our industry, and venturing into the next chapter of Moore's law in the context of upcoming IC ecosystems.

Panelists:	**Chenming Hu**, *University of California, Berkeley, CA*
	H.-S. Philip Wong, *Stanford University, Stanford, CA*
	Mendy Furmanek, *IBM, Dallas, TX*
	Ian Young, *Intel, Hillsboro, OR*
	Isabelle Ferain, *Global Foundries, Dresden, Germany*

Machine Learning Accelerators

Session Chair: **Chia-Hsiang Yang,** *National Taiwan University, Taipei, Taiwan*
Session Co-Chair: Ji-Hoon Kim, *Ewha Womans University, Seoul, Korea*

8:00 AM

20.1 NVE: A 3nm 23.2TOPS/W 12b-Digital-CIM-Based Neural Engine for High-Resolution Visual-Quality Enhancement on Smart Devices

M-E. Shih*[1], S-W. Hsieh*[1], P-Y. Tsai*[1], M-H. Lin[1], P-K. Tsung[1], E-J. Chang[1], J. Liang[1], S-H. Chang[1], C-L. Huang[1], Y-Y. Nian[1], Z. Wan[2], S. Kumar[2], C-X. Xue[1], G. Jedhe[2], H. Fujiwara[3], H. Mori[3], C-W. Chen[1], P-H. Huang[1], C-F. Juan[1], C-Y. Chen[1], T-Y. Lin[1], C. Wang[1], C-C. Chen[1], K. Jou[1]
[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, San Jose, CA
[3]TSMC, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

8:25 AM

20.2 A 28nm 74.34TFLOPS/W BF16 Heterogenous CIM-Based Accelerator Exploiting Denoising-Similarity for Diffusion Models

R. Guo[1], L. Wang[1], X. Chen[1], H. Sun[1], Z. Yue[1], Y. Qin[1], H. Han[1], Y. Wang[1], F. Tu[2], S. Wei[1], Y. Hu[1], S. Yin[1]
[1]Tsinghua University, Beijing, China
[2]Hong Kong University of Science and Technology, Hong Kong, China

8:50 AM

20.3 A 23.9TOPS/W @ 0.8V, 130TOPS AI Accelerator with 16× Performance-
DS2 Accelerable Pruning in 14nm Heterogeneous Embedded MPU for Real-Time Robot Applications

K. Nose, T. Fujii, K. Togawa, S. Okumura, K. Mikami, D. Hayashi, T. Tanaka, T. Toi
Renesas Electronics, Tokyo, Japan

9:15 AM

20.4 A 28nm Physics Computing Unit Supporting Emerging Physics-Informed Neural Network and Finite Element Method for Real-Time Scientific Computing on Edge Devices

Y. Ju, G. Xu, J. Gu
Northwestern University, Evanston, IL

Break 9:40 AM
10:05 AM

20.5 C-Transformer: A 2.6-to-18.1µJ/Token Homogeneous DNN-
DS2 Transformer/Spiking-Transformer Processor with Big-Little Network and Implicit Weight Generation for Large Language Models

S. Kim, S. Kim, W. Jo, S. Kim, S. Hong, H-J. Yoo
Korea Advanced Institute of Science and Technology, Daejeon, Korea

10:30 AM

20.6 LSPU: A Fully Integrated Real-Time LiDAR-SLAM SoC with Point-Neural-
DS2 Network Segmentation and Multi-Level kNN Acceleration

J. Jung[1], S. Kim[1], B. Seo[1], W. Jang[1], S. Lee[1], J. Shin[1], D. Han[2], K. J. Lee[1]
[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]Massachusetts Institute of Technology, Cambridge, MA

10:55 AM

20.7 NeuGPU: A 18.5mJ/Iter Neural-Graphics Processing Unit for Instant-
DS2 Modeling and Real-Time Rendering with Segmented-Hashing Architecture

J. Ryu[1], H. Kwon[1], W. Park[1], Z. Li[1], B. Kwon[1], D. Han[2], D. Im[1], S. Kim[1], H. Joo[1], H-J. Yoo[1]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Massachusetts Institute of Technology, Cambridge, MA

11:20 AM

20.8 Space-Mate: A 303.5mW Real-Time Sparse Mixture-of-Experts-Based
DS2 NeRF-SLAM Processor for Mobile Spatial Computing

G. Park[1], S. Song[1], H. Sang[1], D. Im[1], D. Han[2], S. Kim[1], H. Lee[1], H-J. Yoo[1]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Massachusetts Institute of Technology, Cambridge, MA

Conclusion 11:45 AM

TIMETABLE OF ISSCC 2024 SESSIONS

ISSCC 2024 • SUNDAY, FEBRUARY 18TH

TUTORIALS

8:30 AM	**T1:** Process-Scalable Low-Power Amplifiers	**T2:** Fundamentals of Digital and Digitally Assisted Linear Voltage Regulators	**T3:** Fundamentals of Circuit Design for 2.5D/3D Integration
10:30 AM	**T4:** Fundamentals of Power Management Systems: Constraints and Solutions	**T5:** Calibration Techniques in PLLs	**T6:** Recent Circuit Advances for Resilience to Side-Channel Attacks
1:30 PM	**T7:** Fundamentals of Continuous-Time ADCs	**T8:** 3D Flash Memory from Technology to the System: Past, Present and Future Developments	
3:30 PM	**T9:** Domain-Specific Accelerators: From Hardware to Systems	**T10:** Fundamentals of Transceivers for Communication and Sensing	

FORUMS

8:00 AM	**F1:** Efficient Chiplets and Die-to-Die Communications	**F2:** Energy-Efficient AI-Computing Systems for Large-language Models

EVENTS BELOW IN BOLD BOX ARE INCLUDED WITH YOUR CONFERENCE REGISTRATION

EVENING EVENTS

4:00 PM: Mentoring Session / Networking Bingo Event	**8:00 PM EE1:** Student Research Preview Short Presentations with Poster Session

ISSCC 2024 • MONDAY, FEBRUARY 19TH • PAPER SESSIONS

8:30 AM	**SESSION 1:** PLENARY SESSION				
1:30 PM	**Session 2:** Processors and Communication SoCs	**Session 3:** Analog Techniques	**Session 4:** High Performance Transceivers and Transmitters for Communication and Ranging / **3:35 PM – Session 5:** Wireless RF and mm-Wave Receiver Techniques	**Session 6:** Imagers and Ultrasound	**Session 7:** Ultra-High-Speed Wireline

3:00 PM to 8:00 PM – Book Displays • Corporations/Institution Exhibition

5:00 PM to 7:00 PM – Demonstration Session • 5:30 PM – Author Interviews • Social Hour

EVENING EVENTS

8:00 PM	**EE2:** Career Trajectories: Sharing our Paths to Success	**EE3:** Mixed-Foundry Chiplets? Opportunities and Challenges

ISSCC 2024 • TUESDAY, FEBRUARY 20TH • PAPER SESSIONS

8:00 AM	**Session 8:** Hybrid DC-DC Converters	**Session 9:** Noise Shaping and SAR ADCs	**Session 10:** Frequency Synthesis	**Session 11:** Industry Invited / **10:05 AM – Session 12:** Electromagnetic Interface ICs for Information and Power	**Session 13:** High-Density Memory and Interfaces
1:30 PM	**Session 14:** Digital Techniques for System Adaptation, Power Management and Clocking	**Session 15:** Embedded Memories & Ising Computing	**Session 16:** Security: From Processors to Circuits	**Session 17:** Emerging Sensing and Computing Technologies	**Session 18:** High-Performance Optical Transceivers / **3:35 PM – Session 19:** RF to mm-Wave Oscillators and Multipliers

9:30 AM to 1:30 PM; and from 3:00 PM to 8:00 PM – Book Displays • Corporations/Institution Exhibition

5:00 PM to 7:00 PM – Demonstration Session • 5:30 PM – Author Interviews • Social Hour

EVENING EVENTS

8:00 PM	**EE4:** Generative AI for Chip Design	**EE5:** The Legacy of Gordon Moore

ISSCC 2024 • WEDNESDAY, FEBRUARY 21ST • PAPER SESSIONS

8:00 AM	**Session 20:** Machine Learning Accelerators	**Session 21:** Audio Amplifiers / **10:05 AM – Session 22:** High-Speed Analog-to-Digital Converters	**Session 23:** Energy-Efficient Connectivity Radios / **10:05 AM – Session 24:** D-Band/Sub-THz Transmitters and Sensors	**Session 25:** Invited: Innovations from Outside the (ISSCC's) Box / **10:05 AM – Session 26:** Display and User Interaction Technologies	**Session 27:** Wireless Power / **10:05 AM – Session 28:** High-Density Power Management
1:30 PM	**Session 29:** ICs for Quantum Technologies / **3:35 PM – Session 30:** Domain-Specific Computing and Digital Accelerators	**Session 31:** Power Converter Techniques	**Session 32:** Power Amplification and Signal Generation	**Session 33:** Intelligent Neural Interfaces and Sensing Systems	**Session 34:** Compute-In-Memory

10:00 AM to 3:00 PM – Book Displays • 5:30 PM – Author Interviews

ISSCC 2024 • THURSDAY, FEBRUARY 22ND

8:00 AM	**Short Course:** Machine Learning Hardware: Considerations and Accelerator Approaches	**F3:** Digitally Enhanced Analog Circuits: Trends & State-of-the-art Designs	**F4:** Intelligent Sensing	**F5:** Recent Developments in High-Performance Frequency Synthesis Circuits and Systems	**F6:** Toward Next Generation of Highly Integrated Electrical and Optical Transceivers

Audio Amplifiers

Session Chair: **Shon-Hang Wen,** *Mediatek, Hsinchu, Taiwan*
Session Co-Chair: **Chinwuba Ezekwe,** *Robert Bosch, Sunnyvale, CA*

8:00 AM

21.1 A 121.7dB DR and -109.0dB THD+N Filterless Digital-Input Class-D Amplifier with an HV Multibit IDAC Using Tri-level Output and Employing a Transition-Rate-Balanced Bidirectional RTDEM Scheme

H. Zhang[1], M. Zhang*[1], M. Chen[1], A. Admiraal[1], M. Zhang[1], M. Berkhout[2], Q. Fan[1]*
[1]Delft University of Technology, Delft, The Netherlands
[2]Goodix Technology, Nijmegen, The Netherlands
*Equally Credited Authors (ECAs)

8:25 AM

21.2 A 0.81mA, -105.2dB THD+N Class-D Audio Amplifier with Capacitive Feedforward and PWM-Aliasing Reduction for Wide-Band-Effective Linearity Improvement

K. Zhou, J. Zhou, Y. Tang, J. Li, Z. Hong, J. Xu
Fudan University, Shanghai, China

8:50 AM

21.3 A -106.3dB THD+N Feedback-After-LC Class-D Audio Amplifier Employing Current Feedback to Enable 530kHz LC-Filter Cut-Off Frequency

H. Zhang[1], H. Fan[1], M. Zhang[1], M. Berkhout[2], Q. Fan[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Goodix Technology, Nijmegen, The Netherlands

9:15 AM

21.4 A -108dBc THD+N, 2.3mW Class-H Headphone Amplifier with Power-Aware SIMO Supply Modulator

S-H. Wen, C-H. Hsiao*, Y-W. Huang*, K-Y. Lin, Y-S. Chen, Y-C. Chen, M-C. Tsai, K-H. Chen, K-D. Chen*
MediaTek, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

Break 9:40 AM

High-Speed Analog-to-Digital Converters

Session Chair: **Pieter Harpe,** *Eindhoven University of Technology,*
Eindhoven, The Netherlands
Session Co-Chair: **Benjamin Hershberg,** *Intel, Portland, OR*

10:05 AM

22.1 A 12GS/s 12b 4× Time-Interleaved Pipelined ADC with Comprehensive Calibration of TI Errors and Linearized Input Buffer

Y. Cao[1], M. Zhang[1], Y. Zhu[1], R. P. Martins[1,2], C-H. Chan[1]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

10:30 AM

22.2 A 700MHz-BW −164dBFS/Hz-Small-Signal-NSD 703mW Continuous-Time Pipelined ADC with On-Chip Digital Reconstruction Achieving <−85dBFS HD$_3$ Using Digital Cancellation of DAC Errors

S. Patil[1], A. Ganesan[1], H. Shibata[1], V. Kozlov[1], G. Taylor[2], Q. Yu[3], Z. Li[1], Z. Lulec[1], K. Vasilakopoulos[1], P. Shrestha[2], D. Paterson[4], R. Theertham[1], A. Chowdhury[5]
[1]Analog Devices, Toronto, Canada
[2]Analog Devices, San Diego, CA
[3]now with Amazon, Toronto, Canada
[4]Analog Devices, Wilmington, MA
[5]now with University of Toronto, Toronto, Canada

10:55 AM

22.3 A 76mW 40GS/s 7b Time-Interleaved Hybrid Voltage/Time-Domain ADC with Common-Mode Input Tracking

A. Whitcombe[1], S. Kundu[2,4], H. Chandrakumar[2], A. Agrawal[2], T. Brown[2], S. Callender[3], B. Carlton[2], S. Pellerano[2]
[1]Intel, Santa Clara, CA
[2]Intel, Hillsboro, OR
[3]Intel, Fort Collins, CO
[4]now with AMD, Hillsboro, OR

11:20 AM

22.4 A 4.8GS/s 7-ENoB Time-Interleaved SAR ADC with Dither-Based Background Timing-Skew Calibration and Bit-Distribution-Based Background Ping-Pong Comparator Offset Calibration

Y. Tao, M. Gu, B. Chi, Y. Zhong, L. Jie, N. Sun
Tsinghua University, Beijing, China

11:45 AM

22.5 A 42GS/s 7b 16nm Massively Time-Interleaved Slope-ADC

E. Martens[1], A. Cooman[1], P. Renukaswamy[1], S. Nagata[2], S. Park[1], J. Lagos[1], N. Markulic[1], J. Craninckx[1]
[1]imec, Heverlee, Belgium
[2]Sony Semiconductor Solutions, Atsugi, Japan

Conclusion 12:00 PM

Energy-Efficient Connectivity Radios

Session Chair: **Renzhi Liu,** *Intel, Hillsboro, OR*
Session Co-Chair: **Giuseppe Gramegna,** *IMEC, Golfe Juan, France*

8:00 AM

23.1 A 44µW IoT Tag Enabling 1µs Synchronization Accuracy and OFDMA Concurrent Communication with Software-Defined Modulation

J. Shen [*1], F. Zhu* [*2], Y. Liu[1], B. Liu[1], C. Shi[1], L. Huang[1], L. Xu[1], X. Tian[2], R. Zhang[1]*
[1]East China Normal University, Shanghai, China
[2]Shanghai Jiao Tong University, Shanghai, China
*Equally Credited Authors (ECAs)

8:25 AM

23.2 A 1mm² Software-Defined Dual-Mode Bluetooth Transceiver with 10dBm
DS2 Maximum TX Power and -98.2dBm Sensitivity 2.96mW RX Power at 1Mb/s

N. Scolari, F. X. Pengg, K. Manetakis, C. A. Salazar, A. Vouilloz, E. Pérez Serna, A. Dissanayake, P. Persechini, V. Kopta, E. Le Roux, F. Chicco, S. Cillo, N. Gerber, C. Barbelenet, F. Epifano, P. A. Dal Fabbro, N. Raemy
CSEM, Neuchâtel, Switzerland

8:50 AM

23.3 A Passive Crystal-Less Wi-Fi-to-BLE Tag Demonstrating Battery-Free FDD Communication with Smartphones

Z. Chang [*1], Q. Xiao* [*1], C. Chen[2], W. Wang[1], X. Hu[1], C. Yang[1], Z. Li[1], Y. Luo[1], B. Zhao[1]*
[1]Zhejiang University, Hangzhou, China
[2]Microaiot, Hangzhou, China
*Equally Credited Authors (ECAs)

9:15 AM

23.4 A 167µW 71.7dB-SFDR 2.4GHz BLE Receiver Using a Passive Quadrature-Front-End, a Double-Sided Double-Balanced Cascaded Mixer and a Dual-Transformer-Coupled Class-D VCO

H. Shao[1], R. P. Martins[1,2], P-I. Mak[1]
[1]University of Macau, Macau, China
[2]University of Lisboa, Lisboa, Portugal

9:30 AM

23.5 A 7.6mW IR-UWB Receiver Achieving –13dBm Blocker Resilience with
DS2 a Linear RF Front-End

A. N. Bhat, P. Mateman, Z. Xu, P. Vis, P. Detterer, G. K. Ramachandra, Y. Baykal, M. Konijnenburg, Y-H. Liu, C. Bachmann, P. Zhang
imec, Eindhoven, The Netherlands

Break 9:45 AM

D-Band/Sub-THz Transmitters and Sensors

Session Chair: **Bodhisatwa Sadhu,** *IBM T. J. Watson Research Center,*
Yorktown Heights, NY
Session Co-Chair: **Shahriar Shahramian,** *Nokia – Bell Labs,*
New Providence, NJ

24.1 A 90-to-180GHz APD-Integrated Transmitter Achieving 18dBm P_{sat} in
DS2 28nm CMOS

D. Tang[1], X. Xia[1], Z. Yan[1], P. Zhou[1], Z. Li[1], C. Yang[1], R. Zhang[1], Z. Chen[1], J. Chen[1],
H. Gao[1,2], W. Hong[1]
[1]Southeast University, Nanjing, China
[2]Eindhoven University of Technology, Eindhoven, The Netherlands

24.2 A Scalable 134-to-141GHz 16-Element CMOS 2D λ/2-Spaced Phased
Array

J. Zhang*, B. Dai*, X. Meng, Y. Hu, M. Guan, H. Deng, B. Zhang, C. Wang
University of Electronic Science and Technology of China, Chengdu, China
*Equally Credited Authors (ECAs)

24.3 A 236-to-266GHz 4-Element Amplifier-Last Phased-Array Transmitter in
65nm CMOS

C. Wang[1], H. Herdian[1], W. Zheng[1], C. Liu[1], J. Mayeda[1], Y. Liu[1], O. A. Yong[1], W. Wang[1],
Y. Zhang[1], C. D. Gomez[1], A. Shehata[1], S. Kato[1], I. Abdo[2], T. Jyo[2], H. Hamada[2],
H. Takahashi[2], H. Sakai[1], A. Shirane[1], K. Okada[1]
[1]Tokyo Institute of Technology, Tokyo, Japan
[2]Nippon Telegraph and Telephone, Tokyo, Japan

24.4 Sub-THz Ruler: Spectral Bistability in a 235GHz Self-Injection-Locked
Oscillator for Agile and Unambiguous Ranging

S. M. H. Naghavi[1,2], M. Tavakoli Taba[1,3], A. Tabatabavakili[1], A. Mostajeran[1,4],
M. Aseeri[5], A. Cathelin[6], E. Afshari[1]
[1]University of Michigan, Ann Arbor, MI
[2]now at The University of Washington, Seattle, WA
[3]now at Apple, Cupertino, CA
[4]now at Zadar Labs, San Jose, CA
[5]King Abdulaziz City for Science and Technology, Riyadh, Saudi Arabia
[6]STMicroelectronics, Crolles, France

Conclusion 11:45 AM

Invited: Innovations from Outside the (ISSCC's) Box

Session Chair: **Firooz Aflatouni,** *University of Pennsylvania, Philadelphia, PA*
Session Co-Chair: **Kaushik Sengupta,** *Princeton University, Princeton, NJ*

8:00 AM

25.1 **Short-Reach Silicon Photonic Interconnects with Quantum Dot Mode Locked Laser Comb Sources**
A. Netherton[1], M. Dumont[1], Z. Nelson[1], J. Jhonsa[1], A. Mo[1], J. Koo[1], D. McCarthy[1], N. Pestana[2], S. Deckoff-Jones[2], C. Poulton[2], M. Frankel[3], J. Bovington[4], L. Theogarajan[1], J. Bowers[1]
[1]University of California, Santa Barbara, CA
[2]Analog Photonics, Boston, MA
[3]Ciena, Hanover, MD
[4]Cisco Optical, Nuremberg, Germany

8:25 AM

25.2 **Extreme Wave-Based Metastructures**
N. Engheta
University of Pennsylvania, Philadelphia, PA

8:50 AM

25.3 **Toward Exponential Growth of Therapeutic Neurotechnology**
J. T. Robinson[1,2], J. E. Woods[1], K. Yang[1]
[1]Rice University, Houston, TX
[2]Motif Neurotech, Houston, TX

9:15 AM

25.4 **Liquid Metal – Polymer Composites for Stretchable Circuits, Soft Machines, and Thermal Management**
C. Majidi
Carnegie Mellon University, Pittsburgh, PA

Break 9:40 AM

Display and User Interaction Technologies

Session Chair: Mutsumi Hamaguchi, *Sharp Corporation, Nara, Japan*
Session Co-Chair: Leonardo Gasparini, *Fondazione Bruno Kessler,Trento, Italy*

10:05 AM

26.1 A 600ch 10b Source-Driver IC with a Charge-Modulation DAC Achieving 1-Horizontal Time of 1.5μs Suitable for 240Hz-Frame-Rate Mobile Displays

Y. Park[1], G-G. Kang[1], G-W. Lim[1], S. Shin[1], Y-S. Ahn[2], W. Kim[2], H-S. Kim[1]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]LX Semicon, Seoul, Korea

10:30 AM

26.2 A Fully Nonlinear Compact 10b Source Driver with Low-Voltage Gamma Slope DAC and Data/Phase Dependent Current Modulation Achieving 2411μm²/Channel for Mobile OLED Displays

J. Ahn[1], S. H. Choi[1], J. An[1], K-D. Kim[2], H-M. Lee[1]
[1]Korea University, Seoul, Korea
[2]C&Tech, Seoul, Korea

10:55 AM

26.3 Noise Immunity in Capacitive Sensing: Single-Ended AFE Design with Common-Current Subtraction for Mutual- and Self-Capacitance Sensing in 390pF Load

J. Y. An[1], S. H. Choi[1], S-W. Kim[2], J-Y. Lee[2], H-M. Lee[1], Y-K. Choi[1]
[1]Korea University, Seoul, Korea
[2]Samsung Electronics, Hwaseong, Korea

11:20 AM

26.4 A 620pF-Compensated Dual-Mode Capacitance Readout IC for Sub-Display TSP with VRR Scan

J. Lee*[1], J. Ham*[1], H. Lee[1], W. Jang[1], H. Kim[2], B. So[2], S. Ko[1]
[1]Kwangwoon University, Seoul, Korea
[2]Zinitix, Suwon, Korea
*Equally Credited Authors (ECAs)

11:45 AM

26.5 A 977μW Capacitive Touch Sensor with Noise-Immune Excitation Source
DS2 and Direct Lock-In ADC Achieving 25.2pJ/step Energy Efficiency

X. Feng[1], Z. Wang[1], Y. Chen[1], T. Cai[1], Y. Xuan[1], C. Yang[1], W. Wang[1], Y. Zhang[2], Z. Tang[3], Y. Luo[1], B. Zhao[1]

[1]Zhejiang University, Hangzhou, China
[2]Microaiot, Hangzhou, China
[3]Vango Technologies, Hangzhou, China

Conclusion 12:00 PM

Wireless Power

Session Chair: **Patrik Arno,** *ST Microelectronics, Grenoble, France*
Session Co-Chair: **Kousuke Miyaji,** *Shinshu University, Nagano, Japan*

8:00 AM

27.1   A Differential Hybrid Class-ED Power Amplifier with 27W Maximum Power and 82% Peak E2E Efficiency for Wireless Fast Charging To-Go
F. Mao, R. Martins, Y. Lu
University of Macau, Macau, China

8:25 AM

27.2   A 6.78MHz 79.5%-Peak-Efficiency Wireless Power Transfer System Using a Wireless Mode-Recognition Technique and a Fully-On/off Class-D Power Amplifier
J. Ge, Y. Lu, R. Yang, D. Pan, L. Cheng
University of Science and Technology of China, Hefei, China

8:50 AM

27.3   A 90.8%-Efficiency SIMO Resonant Regulating Rectifier Generating 3 Outputs in a Half Cycle with Distributed Multi-Phase Control for Wirelessly-Powered Implantable Devices
H-S. Lee, K. Eom, H-M. Lee
Korea University, Seoul, Korea

9:15 AM

27.4   A 13.56MHz Wireless Power Transfer System with Hybrid Voltage-/Current-Mode Receiver and Global Digital-PWM Regulation Achieving 150% Transfer Range Extension and 72.3% End-to-End Efficiency
T. Lu, S. Du
Delft University of Technology, Delft, The Netherlands

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27.5   A Wireless Power Transfer System with Up-to-27.9% Efficiency Improvement Under Coupling Coefficient Ranging from 0.1 to 0.39 Based on Phase-Shift/Time-Constant Detection and Hybrid Transmission Power Control
Y. Chen, Y. Luo, Y. Lin, L. Shao, D. Chen, J. Guo
Sun Yat-Sen University, Guangzhou, China

Break 9:45 AM

High-Density Power Management

Session Chair: **Xun Liu,** *Chinese University of Hong Kong,*
Shenzhen, China
Session Co-Chair: **Hanh-Phuc Le,** *University of California,*
San Diego, La Jolla, CA

10:05 AM

28.1 A Fully Integrated, Domino-Like-Buffered Analog LDO Achieving −28dB Worst-Case Power-Supply Rejection Across the Frequency Spectrum from 10Hz to 1GHz with 50pF On-Chip Capacitance

J-G. Lee[1], H-H. Bae[1], S. Jang[2], H-S. Kim[1]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]Electronics and Telecommunications Research Institute, Daejeon, Korea

10:30 AM

28.2 A 12V-Input 1V-1.8V-Output 94.7%-Peak-Efficiency 685A/cm³-Current-Density Hybrid DC-DC Converter with a Charge Converging Phase

Y. Ji, J. Jin, L. Cheng
University of Science and Technology of China, Hefei, China

10:55 AM

28.3 A 12-28V to 0.6-1.8V Ratio-Regulatable Dickson SC Converter with Dual-Mode Phase Misalignment Operations Achieving 93.1% Efficiency and 6A Output

Q. Ma[1], Y. Jiang[1], H. Li[1], X. Zhang[1], M-K. Law[1], R. P. Martins[1,2], P-I. Mak[1]
[1]University of Macau, Macau, China
[2]University of Lisboa, Lisbon, Portugal

11:20 AM

28.4 A Monolithic 12.7W/mm²-Pmax, 92% Peak-Efficiency CSCR-First Switched-Capacitor DC-DC Converter

N. Butzen, H. Krishnamurthy, J. Yu, Z. K. Ahmed, S. Weng, K. Ravichandran, R. H. Ahangharnejhad, J. Waldemer, C. Pelto, J. Tschanz
Intel, Hillsboro, OR

11:35 AM

28.5 A 94.1%-Efficiency Parallel-SC Hybrid Buck Converter Designed Using VCR-Aware Topology Optimizer for a 4.2A/mm² Current-Density FoM

H. Han, J-H. Cho, W. Jang, Y. Park, J. Lee, H-S. Kim
Korea Advanced Institute of Science and Technology, Daejeon, Korea

11:50 AM

28.6 An 87% Efficient 2V-Input, 200A Voltage Regulator Chiplet Enabling
DS2 **Vertical Power Delivery in Multi-kW Systems-on-Package**

R. Jain[1], S. Xu[2], R. Kaushal[1], C. Mariscal[1], H. Caballero[3], T. Salus[4], C. Schaef[1], A. Deka[5], A. Payala[5], K. Chen[6], H. Do[7], J. Douglas[7]
[1]Intel, Hillsboro, OR
[2]Intel, Santa Clara, CA
[3]Intel, Guadalajara, Mexico
[4]Intel, Haifa, Israel
[5]Intel, Bangalore, India
[6]Intel, Hudson, MA
[7]Intel, Chandler, AZ

Conclusion 12:05 PM

ICs for Quantum Technologies

Session Chair: **Giorgio Ferrari,** *Politecnico di Milano, Milano, Italy*
Session Co-Chair: **Joseph Bardin,** *Google & UMass Amherst, Goleta, CA*

1:30 PM

29.1 A 22nm FD-SOI <1.2mW/Active-Qubit AWG-Free Cryo-CMOS Controller for Fluxonium Qubits

L. Le Guevel[1], C. Wang[1], J. C. Bardin[1,2]
[1]University of Massachusetts, Amherst, MA
[2]Google Quantum AI, Goleta, CA

1:55 PM

29.2 A Cryo-CMOS Controller with Class-DE Driver and DC Magnetic-Field Tuning for Color-Center-Based Quantum Computers

L. Enthoven*[1], N. Fakkel*[1], H. Bartling[2], M. van Riggelen[2], K-N. Schymik[2], J. Yun[2], E. Tsapanou Katranara[2], R. Vollmer[2], T. Taminiau[2], F. Sebastiano**[1], M. Babaie**[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]QuTech, Delft, The Netherlands
*Equally Credited Authors (ECAs)
**Equally Credited Authors (ECAs)

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29.3 A Cryo-CMOS Receiver with 15K Noise Temperature Achieving 9.8dB SNR in 10μs Integration Time for Spin Qubit Readout

B. Prabowo[1,2], O. Pietx-Casas[1,2], M. A. Montazerolghaem[1], G. Scappucci[1,2], L. M.K. Vandersypen[1,2], F. Sebastiano[1,2], M. Babaie[1,2]
[1]Delft University of Technology, Delft, The Netherlands
[2]QuTech, Delft, The Netherlands

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29.4 A Cryo-CMOS Quantum Computing Unit Interface Chipset in 28nm Bulk CMOS with Phase-Detection Based Readout and Phase-Shifter-Based Pulse Generation

Y. Guo[1,2], Q. Liu[3], W. Huang[1], Y. Li[1], T. Tian[1], N. Wu[1], S. Zhang[1], T. Li[1,3], Z. Wang[1], N. Deng[1], Y. Zheng[2], H. Jiang[1]
[1]Tsinghua University, Beijing, China
[2]Nanyang Technological University, Singapore, Singapore
[3]Beijing Academy of Quantum Information Sciences, Beijing, China

3:00 PM

29.5 A Portable 14GHz Dual-Mode Pulse and Continuous-Wave Electron Paramagnetic Resonance Spectrometer Using a Subharmonic Direct Conversion Receiver
DS2

J-H. Sun, M. Rustom, T. D. Nguyen, J. Singh, P. Qin, C. Sideris
University of Southern California, Los Angeles, CA

Break 3:15 PM

Domain-Specific Computing and Digital Accelerators

Session Chair: **Huichu Liu,** *Meta Reality Labs, Sunnyvale, CA*
Session Co-Chair: **Jae-sun Seo,** *Cornell Tech, New York, NY*

3:35 PM

30.1 A 40nm VLIW Edge Accelerator with 5MB of 0.256pJ/b RRAM and a
`DS2` Localization Solver for Bristle Robot Surveillance

S. D. Spetalnick*[1], A. S. Lele*[1], B. Crafton[1], M. Chang[1], S. Ryu[1], J-H. Yoon[2], Z. Hao[1], A. Ansari[1], W-S. Khwa[3], Y-D. Chih[4], M-F. Chang[3], A. Raychowdhury[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea
[3]TSMC Corporate Research, Hsinchu, Taiwan
[4]TSMC Design Technology, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

4:00 PM

30.2 A 22nm 0.26nW/Synapse Spike-Driven Spiking Neural Network
Processing Unit Using Time-Step-First Dataflow and Sparsity-Adaptive
In-Memory Computing

Y. Liu*[1], Y. Ma*[1], N. Shang[1], T. Zhao[2], P. Chen[1], M. Wu[1], J. Ru[1], T. Jia[1], L. Ye[1], Z. Wang[3], R. Huang[1]
[1]Peking University, Beijing, China
[2]Nano Core Chip Electronic Technology, Hangzhou, China
[3]Beijing Information Science and Technology University, Beijing, China
*Equally Credited Authors (ECAs)

4:25 PM

30.3 VIP-Sat: A Boolean Satisfiability Solver Featuring 5×12 Variable In-
Memory Processing Elements with 98% Solvability for 50-Variables
218-Clauses 3-SAT Problems

C. Shim, J. Bae, B. Kim
University of California, Santa Barbara, CA

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30.4 A Fully Integrated Annealing Processor for Large-Scale Autonomous
Navigation Optimization

Y-C. Chu, Y-C. Lin, Y-C. Lo, C-H. Yang
National Taiwan University, Taipei, Taiwan

5:05 PM

30.5 A Variation-Tolerant In-eDRAM Continuous-Time Ising Machine
Featuring 15-Level Coefficients and Leaked Negative-Feedback
Annealing

J. Song*, Z. Wu*, X. Tang, B. Xu, H. Luo, Y. Yang, Y. Wang, R. Wang, R. Huang
Peking University, Beijing, China
*Equally Credited Authors (ECAs)

5:20 PM

30.6 Vecim: A 289.13GOPS/W RISC-V Vector Co-Processor with Compute-in-
`DS2` Memory Vector Register File for Efficient High-Performance Computing

Y. Wang, M. Yang, C-P. Lo, J. P. Kulkarni
University of Texas, Austin, TX

Conclusion 5:35 PM

Power Converter Techniques

Session Chair: **Saurav Bandyopadhyay,** *Texas Instruments, Dallas, TX*
Session Co-Chair: **Dongsu Kim,** *Samsung Electronics, Hwasung-si, Korea*

1:30 PM

31.1 An 83.4%-Peak-Efficiency Envelope-Tracking Supply Modulator Using a Class-G Linear Amplifier and a Single-Inductor Dual-Input-Dual-Output Converter for 200MHz Bandwidth 5G New Radio RF Applications
C. Chen, X. Li, R. Hu, L. Cheng, University of Science and Technology of China, Hefei, China

1:55 PM

31.2 A Ripple-Less Buck Converter with Sub -21.94dB EVM for 5G Low Earth Orbit Application
Y-H. Kao[1], J-L. Wu[1], W-C. Huang[1], H-H. Chang[1], H-Y. Tsai[1], R-B. Guo[1], K-H. Chen[1], K-L. Zeng[1,2], Y-H. Lin[3], S-R. Lin[3], T-Y. Tsai[3]
[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]Chip-GaN Power Semiconductor, Hsinchu, Taiwan; [3]Realtek Semiconductor, Hsinchu, Taiwan

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31.3 A 950ns 0.5-to-5.5V 5G NR RF PA Supply Modulator with Floating Capacitor Control for Symbol Power Tracking
I-H. Kim, J-I. Seo, Y. Choo, S. Park, J. Han, W. Kim, S. Jung, T. Ko, D. Kim, J. Lee, S. Kwak
Samsung Electronics, Hwaseong, Korea

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31.4 98.7% Efficiency 1200V-to-48V LLC Converter with CC/CV Mode Charging Compliant with EVSE Level 1
T-W. Wang[1], S-H. Hung[1], P-J. Chiu[1], C-Y. Chen[1], C-L. Go[1], Y-T. Huang[1], X-Q. Wu[1], K-H. Chen[1], K-L. Zeng[1,2], Y-H. Lin[3], S-R. Lin[3], T-Y. Tsai[3]
[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]Chip-GaN Power Semiconductor, Hsinchu, Taiwan; [3]Realtek Semiconductor, Hsinchu, Taiwan

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31.5 **A 750-mW, 37% Peak Efficiency Isolated DC-DC Converter with 54/18-Mb/s**
DS2 **Full-Duplex Communication Using a Single Pair of Transformers**
T. Hu[1], M. Huang[1], R. P. Martins[1,2], Y. Lu[1]
[1]University of Macau, Macau, China; [2]University of Lisboa, Lisbon, Portugal

Break 3:15 PM

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31.6 A SIDO/DISO VCF-Step-Reconfigurable Continuously Scalable-Conversion-Ratio SC Converter Achieving 91.4%/92.6% Peak Efficiency and Almost-lossless Channel Switching
Y. Wang[1], M. Huang[1], R. P. Martins[1,2], Y. Lu[1]
[1]University of Macau, Macao, China; [2]University of Lisboa, Lisbon, Portugal

4:00 PM

31.7 A 3.6W 16V-Output 180ns-Response-Time 94%-Efficiency SC Sigma Converter with Output Impedance Compensation and Ripple Mitigation for LiDAR Driver Applications
*C. Hu *[1], X. Huang *[1], X. Liu[2], S. Du[3], X. Liu[4], J. Jiang[1]*
[1]Southern University of Science and Technology, Shenzhen, China
[2]Chinese University of Hong Kong, Shenzhen, China
[3]Delft University of Technology, Delft, The Netherlands; [4]Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

4:25 PM

31.8 A 11.7W 9mV/A-Cross-Regulation Single-Inductor Triple-Output Buck Converter Using Unordered Power-Distributive Control for a 2A Load Transient
B. Wang, X. Wu, L. Cheng, University of Science and Technology of China, Hefei, China

4:50 PM

31.9 An 85-264 Vac to 3-4.2 Vdc 1.05W Capacitive Power Converter with Idle Power Reduction and 4-Phase 1/10X SC Converter Achieving 5.11mW Quiescent Power and 78.2% Peak Efficiency
G. Liu[1,2], H. Wu[1], C. Hu[1], C. Huang[3], X. Liu[2], J. Jiang[1]
[1]Southern University of Science and Technology, Shenzhen, China
[2]Chinese University of Hong Kong, Shenzhen, China; [3]Iowa State University, Ames, IA

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31.10 A Fully Integrated 500V, 6.25MHz GaN-IC for Totem-Pole PFC Off-Line Power Conversion
N. Deneke, B. Wicht, Leibniz University Hannover, Hannover, Germany

5:20 PM

31.11 A Capacitor-Based Bias-Flip Rectifier with Electrostatic Charge Boosting for Triboelectric Energy Harvesting Achieving Auto-MPPT at Breakdown Voltage and 14× Power Extraction Improvement
W. Peng, X. Yue, L. Pakula, S. Du, Delft University of Technology, Delft, The Netherlands

Conclusion 5:35 PM

Power Amplification and Signal Generation

Session Chair: **Ruonan Han,** *Massachusetts Institute of Technology, Cambridge, MA*

Session Co-Chair: **Henrik Sjöland,** *Lund University, Ericsson Research, Lund, Sweden*

1:30 PM

32.1 A 47GHz 4-Way Doherty PA with 23.7dBm P_{1dB} and 21.7% / 13.1% PAE
DS2 at 6 / 12dB Back-Off Supporting 2000MHz 5G NR 64-QAM OFDM
X. Zhang*, H. Guo*, T. Chi, Rice University, Houston, TX
*Equally Credited Authors (ECAs)

1:55 PM

32.2 A 24.25-to-29.5GHz Extremely Compact Doherty Power Amplifier with
Differential-Breaking Phase Offset Achieving 23.7% PAE_{avg} for 5G
Base-Station Transceivers
H. Oh, S. Park, J. Lee, S. Baek, J. Jung, T. Kim, J. Kim, W. Lee, J-H. Park, K. Kim, D-H. Lee, S. Lee, J. H. Lee, J. H. Kim, Y. Kim, S. Park, B. Suh, S. Oh, D. Lee, S. Jeon, J. Son, S-G. Yang, Samsung Electronics, Suwon, Korea

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32.3 A Load-Variation-Tolerant Doherty Power Amplifier with
Dual-Adaptive-Bias Scheme for 5G Handsets
S. Imai, H. Sato, K. Mukai, H. Okabe, Murata, Kyoto, Japan

2:45 PM

32.4 A 67.8-to-108.2GHz Power Amplifier with a Three-Coupled-Line-Based
Complementary-Gain-Boosting Technique Achieving 442GHz GBW and
23.1% peak PAE
W. Wu, X. Bao, S. Chen, Y. Wang, L. Zhang, Tsinghua University, Beijing, China

3:00 PM

32.5 E-band (71-to-86GHz) GaN Power Amplifier with 4.37W Output Power
DS2 and 18.5% PAE for 5G Backhaul
B. Cimbili[1,2,3], M. Bao[2], C. Friesicke[1], R. Quay[1,3], [1]Fraunhofer IAF, Freiburg, Germany
[2]Ericsson, Gothenburg, Sweden; [3]University of Freiburg, Freiburg, Germany

Break 3:15 PM
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32.6 A 76-to-81GHz Direct-Digital 7b 14GS/s Double-Balanced I/Q Mixing-DAC
Radar-Waveform Synthesizer
M. Neofytou[1,2], K. Doris[1,2], M. Ganzerli[1], M. Lont[1], G. I. Radulov[2]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands

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32.7 A 25.2dBm P_{SAT}, 35-to-43GHz VSWR-Resilient Chain-Weaver Eight-Way
Balanced PA with an Embedded Impedance/Power Sensor
M. Pashaeifar, A. K. Kumaran, L. C. de Vreede, M. S. Alavi
Delft University of Technology, Delft, The Netherlands

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32.8 A 27.8-to-38.7GHz Load-Modulated Balanced Power Amplifier with
Scalable 7-to-1 Load-Modulated Power-Combine Network Achieving
27.2dBm Output Power and 28.8%/23.2%/16.3%/11.9% Peak/6/9/12dB
Back-Off Efficiency
W. Zhu[1], J. Ying[1], L. Chen[2], J. Zhang[2], G. Lv[2], X. Yi[2], Z. Zhao[1], Z. Wang[1], Y. Wang[2], W. Chen[2], H. Sun[1]
[1]Beijing Institute of Technology, Beijing, China; [2]Tsinghua University, Beijing, China

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32.9 An Ultra-Compact 28GHz Doherty Power Amplifier with an
Asymmetrically-Coupled-Transformer Output Combiner
E. Liu[1,2], H. Wang[1], [1]ETH Zurich, Zurich, Switzerland
[2]Georgia Institute of Technology, Atlanta, GA

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32.10 A Compact Broadband VSWR-Resilient True Power and Gain Sensor
with Dynamic-Range Compensation for Phased-Array Applications
E. Liu*[1], D. Munzer*[2], J. Lee[2], H. Wang[1]
[1]ETH Zurich, Zurich, Switzerland; [2]Georgia Institute of Technology, Atlanta, GA
*Equally Credited Authors (ECAs)

Conclusion 5:20 PM

Intelligent Neural Interfaces and Sensing Systems

Session Chair: **Jerald Yoo**, *National University of Singapore,*
Singapore, Singapore
Session Co-Chair: **Mehdi Kiani**, *The Pennsylvania State University,*
University Park, PA

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33.1 **A High-Accuracy and Energy-Efficient Zero-Shot-Retraining Seizure-Detection**
DS2 **Processor with Hybrid-Feature-Driven Adaptive Processing and Learning-Based**
Adaptive Channel Selection

J. Liu[1], X. Liu[1], X. Wang[1], Z. Xie[1], Z. Zhong[1], J. Fan[1], H. Qiu[1], Y. Xu[1], H. Qin[1], Y. Long[1], Y. Zhou[2],
Z. Shen[3], L. Zhou[1], L. Chang[1], S. Liu[1], S. Lin[1], C. Wang[3], J. Zhou[1]
[1]University of Electronic Science and Technology of China, Chengdu, China
[2]West China Hospital of Sichuan University, Chengdu, China
[3]Huazhong University of Science and Technology, Wuhan, China

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33.2 **A Sub-1µJ/class Headset-Integrated Mind Imagery and Control SoC for VR/MR**
DS2 **Applications with Teacher-Student CNN and General-Purpose Instruction Set**
Architecture

Z. Zhong*, Y. Wei*, L. C. Go, J. Gu, Northwestern University, Evanston, IL
*Equally Credited Authors (ECAs)

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33.3 **MiBMI: A 192/512-Channel 2.46mm² Miniaturized Brain-Machine Interface Chipset**
Enabling 31-Class Brain-to-Text Conversion Through Distinctive Neural Codes

M. Shaeri[1,2], U. Shin[1,2,3], A. Yadav[1,2], R. Caramellino[4], G. Rainer[1,4], M. Shoaran[1,2]
[1]EPFL, Lausanne, Switzerland; [2]Neuro-X Institute, Geneva, Switzerland
[3]Cornell University, Ithaca, NY; [4]University of Fribourg, Fribourg, Switzerland

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33.4 **A Multi-Loop Neuromodulation Chipset Network with Frequency-Interleaving Front-**
End and Explainable AI for Memory Studies in Freely Behaving Monkeys

Y. Hou[1], Y. Zhu[1], X. Wu[1], Y. Li[1], T. Lucas[2], A. Richardson[3], X. Liu[1]
[1]University of Toronto, Toronto, Canada; [2]Ohio State University, Columbus, OH
[3]University of Pennsylvania, Philadelphia, PA

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33.5 **Closed-Loop 100-Channel Highly-Scalable Retinal Implant with 1.02µW Analog**
ED-Based Adaptive-Threshold Spike Detection and Poisson-Coded Temporally
Distributed Optogenetic Stimulation

T. Yousefi, G. Zoidl, H. Kassiri, York University, Toronto, Canada

Break 3:15 PM
3:35 PM

33.6 **A Millimetric Batteryless Biosensing and Stimulating Implant with Magnetoelectric**
Power Transfer and 0.9pJ/b PWM Backscatter

Z. Yu*, H-C. Liao*, F. Alrashdan, Z. Wen, Y. Zou, J. Woods, W. Wang, J. T. Robinson, K. Yang
Rice University, Houston, TX; **Equally Credited Authors (ECAs)*

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33.7 **An Adhesive Interposer-Based Reconfigurable Multi-Sensor Patch Interface with**
DS2 **On-Chip Application Tunable Time-Domain Feature Extraction**

J. Cho*, Y. J. Pyeon*, J. Yeom*, H. Kim*, S. Cho, Y. Kim, T. Kim, J-H. Kwak, G. Choi, Y. Lee,
H. Shin, H. E. Jeong, J. Kim, Ulsan National Institute of Science and Technology, Ulsan, Korea
*Equally Credited Authors (ECAs)

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33.8 **A Two-Electrode Bio-Impedance Readout IC with Complex-Domain Noise-**
Correlated Baseline Cancellation Supporting Sinusoidal Excitation

S-I. Cheon*[1], H. Choi*[1], G. Yun[1], S. Oh[1], J-H. Suh[1], S. Ha[2], M. Je[1]
[1]Korea Advanced Institute of Science and Technology, Daejeon, Korea
[2]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates
*Equally Credited Authors (ECAs)

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33.9 **A Miniature Neural Interface Implant with a 95% Charging Efficiency Optical**
DS2 **Stimulator and an 81.9dB SNDR ΔΣM-Based Recording Frontend**

L. Zhao[1], W. Shi[2], Y. Gong[3], X. Liu[3], W. Li[3], Y. Jia[1], [1]University of Texas, Austin, TX
[2]Meta, Santa Clara, CA; [3]Michigan State University, East Lansing, MI

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33.10 **A 2.7ps-ToF-Resolution and 12.5mW Frequency-Domain NIRS Readout IC with**
DS2 **Dynamic Light Sensing Frontend and Cross-Coupling-Free Inter-Stabilized Data**
Converter

Z. Ma[1], Y. Lin[1], C. Chen[1], X. Qi[1], Y. Li[1], K-T. Tang[2], F. Wang[3], T. Zhang[4], G. Wang[1], J. Zhao[1]
[1]Shanghai Jiao Tong University, Shanghai, China; [2]National Tsing Hua University, Hsinchu, Taiwan
[3]Shanghai United Imaging Microelectronics Technology, Shanghai, China
[4]Shanghai Mental Health Center, Shanghai, China

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33.11 **A Hybrid Recording System with 10kHz-BW 630mV$_{PP}$ 84.6dB-SNDR**
173.3dB-FOM$_{SNDR}$ and 5kHz-BW 114dB-DR for Simultaneous ExG and Biocurrent
Acquisition

T. Seol, G. Kim, S. Lee, S. Kim, D. Kim, J. Wie, Y. Shin, H. Kang, J. E. Jang, A. K. George, J. Lee
Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

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Compute-In-Memory

Session Chair:　　　**Ankur Agrawal,** *IBM T. J. Watson Research Center,*
　　　　　　　　　　　　　Yorktown Heights, NY
Session Co-Chair:　**Eric Wang,** *TSMC, Hsinchu City, Taiwan*

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34.1　A 28nm 83.23TFLOPS/W POSIT-Based Compute-in-Memory Macro for High-Accuracy AI Applications
Y. Wang, X. Yang, Y. Qin, Z. Zhao, R. Guo, Z. Yue, H. Han, S. Wei, Y. Hu, S. Yin
Tsinghua University, Beijing, China

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34.2　A 16nm 96Kb Integer-Floating-Point Dual-Mode Gain-Cell-Computing-in-Memory Macro Achieving 73.3-163.3TOPS/W and 33.2-91.2TFLOPS/W for AI-Edge Devices
*W-S. Khwa [*1], P-C. Wu [*2], J-J. Wu[1], J-W. Su[2,3], H-Y. Chen[2], Z-E. Ke[2], T-C. Chiu[2], J-M. Hsu[2], C-Y. Cheng[2], Y-C. Chen[2], C-C. Lo[2], R-S. Liu[2], C-C. Hsieh[2], K-T. Tang[2], M-F. Chang[1,2]*
[1]TSMC Corporate Research, Hsinchu, Taiwan; [2]National Tsing Hua University, Hsinchu, Taiwan
[3]Industrial Technology Research Institute, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

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34.3　A 22nm 64kb Lightning-Like Hybrid Computing-in-Memory Macro with Compressed Adder Tree and Analog-Storage Quantizers for Transformer and CNNs
A. Guo[1], X. Chen[1], F. Dong[1], J. Chen[1], Z. Yuan[2,3], X. Hu[3], Y. Zhang[2], J. Zhang[1], Y. Tang[1], Z. Zhang[1], G. Chen[3], D. Yang[3], Z. Zhang[1], L. Ren[1], T. Xiong[1], B. Wang[1], B. Liu[1], W. Shan[1], X. Liu[1], H. Cai[1], G. Sun[2], J. Yang[1], X. Si[1]
[1]Southeast University, Nanjing, China
[2]Peking University, Beijing, China
[3]HOUMO, Beijing, China

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34.4　A 3nm 32.5TOPS/W, 55.0TOPS/mm² and 3.78Mb/mm² Fully-Digital Computing-in-Memory Macro Supporting INT12 x INT12 with a Parallel-MAC Architecture and Foundry 6T SRAM Bit Cell
H. Fujiwara[1], H. Mori[1], W-C. Zhao[1], K. Khare[1], C-E. Lee[1], X. Peng[2], V. Joshi[3], C-K. Chuang[1], S-H. Hsu[1], T. Hashizume[4], T. Naganuma[4], C-H. Tien[1], Y-Y. Liu[1], Y-C. Lai[1], C-F. Lee[1], T-L. Chou[1], K. Akarvardar[2], S. Adham[3], Y. Wang[1], Y-D. Chih[1], Y-H. Chen[1], H-J. Liao[1], T-Y. J. Chang[1]
[1]TSMC, Hsinchu, Taiwan; [2]TSMC, San Jose, CA
[3]TSMC, Ottawa, Canada; [4]TSMC, Yokohama, Japan

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34.5　A 818-4094TOPS/W Capacitor-Reconfigured CIM Macro for Unified Acceleration of CNNs and Transformers
K. Yoshioka, Keio University, Yokohama, Japan

Break 3:15 PM
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34.6 **DS2**　**A 28nm 72.12TFLOPS/W Hybrid-Domain Outer-Product Based Floating-Point SRAM Computing-in-Memory Macro with Logarithm Bit-Width Residual ADC**
Y. Yuan[1,2], Y. Yang[3], X. Wang[3], X. Li[3], C. Ma[1,2], Q. Chen[3], M. Tang[3], X. Wei[3], Z. Hou[3], J. Zhu[1,2], H. Wu[1,2], Q. Ren[1,2], G. Xing[1], P-I. Mak[4], F. Zhang[1]
[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[2]University of Chinese Academy of Sciences, Beijing, China
[3]Beijing Institute of Technology, Beijing, China; [4]University of Macau, Macau, China

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34.7　A 28nm 2.4Mb/mm² 6.9-16.3TOPS/mm² eDRAM-LUT-Based Digital-Computing-in-Memory Macro with In-Memory Encoding and Refreshing
Y. He[1], S. Fan[1], X. Li[1], L. Lei[1], W. Jia[1], C. Tang[1], Y. Li[1], Z. Huang[1], Z. Du[1], J. Yue[2], X. Li[1], H. Yang[1], H. Jia[1], Y. Liu[1]
[1]Tsinghua University, Beijing, China; [2]Chinese Academy of Sciences, Beijing, China

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34.8　A 22nm 16Mb Floating-Point ReRAM Compute-in-Memory Macro with 31.2TFLOPS/W for AI Edge Devices
*T-H. Wen [*1], H-H. Hsu[1,2], W-S. Khwa [*2], W-H. Huang[1], Z-E. Ke[1], Y-H. Chin[1], H-J. Wen[1], Y-C. Chang[1], W-T. Hsu[1], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], S-H. Teng[3], C-C. Chou[3], Y-D. Chih[3], T-Y. J. Chang[3], M-F. Chang[1,2]*
[1]National Tsing Hua University, Hsinchu, Taiwan
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

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34.9　A Flash-SRAM-ADC-Fused Plastic Computing-in-Memory Macro for Learning in Neural Networks in a Standard 14nm FinFET Process
L. Wang[1,2], W. Li[1,2], Z. Zhou[1,2], H. Gao[1,2], Z. Li[1,2], W. Ye[1,2], H. Hu[1], J. Liu[1], J. Yue[1], J. Yang[1], Q. Luo[1], C. Dou[1,2], Q. Liu[1,3], M. Liu[1,3]
[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[2]University of Chinese Academy of Sciences, Beijing, China
[3]Fudan University, Shanghai, China

Conclusion 5:15 PM

Machine Learning Hardware:
Considerations and Accelerator Approaches

Time:	Topic:
8:00 AM	Breakfast
8:25 AM	Introduction by Chair, **Daniel Friedman** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
8:30 AM	**Introduction to Machine Learning Applications and Hardware-Aware Optimizations** **Ranghajaran Venkatesan,** *Nvidia, Santa Clara, CA*
10:00 AM	Break
10:30 AM	**Architecture and Design Approaches to ML Hardware Acceleration: Performance Compute Environment** **Leland Chang,** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
12:15 PM	Lunch
1:20 PM	**Architecture and Design Approaches to ML Hardware Acceleration: Edge and Mobile Environments** **Marian Verhelst,** *KU Leuven, Leuven, Belgium*
2:50 PM	Break
3:20 PM	**Emerging ML Accelerator Approaches: In-Memory Computing Architectures** **Naresh Shanbhag,** *University of Illinois Urbana-Champaign, Champaign, IL*
4:50 PM	Conclusion

Introduction

The growth in the application of machine learning and artificial intelligence technology to problems across virtually all spheres of endeavor has been and is expected to remain extraordinary. Hardware acceleration for machine learning tasks is a critical vector that has enabled this exceptionally rapid growth. Further accelerator advances are necessary to drive everything from improved efficiency for inference, to support ever-growing network sizes to improvements in support for network training, to enabling broadening of ML deployments across platforms with a wide range of power and performance envelopes. In this short course, we will first present an overview of machine learning and inference, including describing key metrics, frameworks, application areas, and approaches to support model scaling. In the second presentation, we will discuss architectural and design approaches to ML hardware acceleration for applications in high performance compute environments. In the third presentation, we will turn to approaches to mapping ML hardware acceleration to constrained compute footprint contexts as in edge and mobile applications. Finally, we will present a framework for considering a key emerging topic in hardware design for ML acceleration, namely, compute-in-memory approaches.

SC1:
Introduction to Machine Learning Applications and Hardware-Aware Optimizations
Ranghajaran Venkatesan, Nvidia, Santa Clara, CA

Deep neural networks (DNNs) have become a crucial solution for tackling complex challenges in a wide range of fields, such as image recognition, natural language processing, robotics, healthcare, and autonomous driving. The landscape of DNN applications is constantly expanding, driving the ongoing evolution of DNN models. These models come in various architectures, including convolutional neural networks, transformers, diffusion models, and more, each tailored to meet the unique demands of their respective applications. These DNN models vary significantly in size and computational complexity, driving the need for efficient neural-network computing chips. This has led to a growing exploration of hardware and software co-design techniques, balancing energy efficiency and performance without compromising accuracy. This short course offers an introductory exploration of different neural network models, shedding light on their individual characteristics and applications. It also delves into various design strategies, emphasizing the importance of achieving a delicate balance between efficiency, scalability, and adaptability across different neural network paradigms, all while paving the way for the emergence of efficient neural network models and computing architectures.

Rangharajan Venkatesan is a Senior Research Scientist in the ASIC & VLSI Research group in NVIDIA. He received the B.Tech. degree in Electronics and Communication Engineering from the Indian Institute of Technology, Roorkee in 2009 and the Ph.D. degree in Electrical and Computer Engineering from Purdue University in 2014. His research interests are in the areas of low-power VLSI design and computer architecture with particular focus in deep learning accelerators, high-level synthesis, and spintronic memories. He has received Best Paper Awards for his work on deep learning accelerators from the IEEE/ACM Symposium on Microarchitecture (MICRO) and the Journal of Solid-State Circuits (JSSC). His work on spintronic memory design was recognized with the Best Paper Award at the International Symposium on Low Power Electronics and Design (ISLPED), and Best Paper nomination at the Design, Automation and Test in Europe (DATE). His paper titled, "MACACO: Modeling and Analysis of Circuits for Approximate Computing", received the IEEE/ACM International Conference on Computer-Aided Design (ICCAD) Ten Year Retrospective Most Influential Paper Award in 2021. He has served as a member of the technical program committees of several leading IEEE/ACM conferences including ISSCC, DAC, MICRO, and ISLPED.

SC2:
Architecture and Design Approaches to ML Hardware Acceleration: Performance Compute Environment
Leland Chang, IBM Thomas J. Watson Research Center, Yorktown Heights, NY

With the recent explosion in generative AI and large language models, hardware acceleration has become particularly important in high-performance compute environments. In such applications, AI accelerators should address a broad range of AI models and enable workflows spanning model pre-training, fine-tuning, and inference. System-level design and software co-optimization must be considered to balance compute and communication costs, especially with inference workloads driving aggressive latency targets and model size growth driving the use of distributed systems. This talk will discuss these considerations in the context of high-performance system deployments and explore approaches to AI accelerator circuit design as well as research roadmaps to improve both compute efficiency and communication bandwidth.

Leland Chang is a Principal Research Scientist and the Senior Manager of AI Hardware at IBM Research, where he leads a team developing AI hardware accelerators for next-generation server and mainframe products. He has worked across technology, circuits, architecture, and software with key technical contributions to FinFET technologies, SRAM scaling, integrated voltage regulators, and AI accelerators. He received the B. S., M. S., and Ph.D. degrees in EECS from UC Berkeley and has authored 100 technical articles and 135 patents. He is a former memory subcommittee chair of the ISSCC technical program committee.

SC3:
Architecture and Design Approaches to ML Hardware Acceleration: Edge and Mobile Environments
Marian Verhelst, KU Leuven, Leuven, Belgium

Various applications demand more and more powerful machine inference in resource-scarce distributed devices, such as phones, watches, glasses, robots or drones. To allow intelligent applications at ultra-low energy and low latency, one needs customized processor architectures optimized for extreme edge applications. This need has resulted in the creation of a wide variety of novel hardware architectures, supported by HW-algorithm co-optimization methods. This talk will zoom into ML processor architectures for the edge, as well as tools for efficient mapping of ML algorithms onto such architectures.

Marian Verhelst is professor at the MICAS laboratories of KU Leuven and a research director at imec. Her research focuses on embedded machine learning, hardware accelerators, HW-algorithm co-design and low-power edge processing. She received a PhD from KU Leuven in 2008, and worked as a research scientist at Intel Labs from 2008 till 2010. Marian currently is a member of the board of directors of tinyML, scientific advisor to multiple startups and active in the TPC's of DATE and ESSCIRC. She enjoys science communication as an IEEE SSCS Distinguished Lecturer, as a regular member of the Nerdland science podcast (Dutch), and as the founding mother of KU Leuven's InnovationLab high school program.

SC4:
Emerging ML Accelerator Approaches: In-Memory Computing Architectures
Naresh Shanbhag, University of Illinois Urbana-Champaign, Champaign, IL

In-memory computing (IMC) has emerged as an attractive complement to digital accelerators for enhancing the energy efficiency of machine learning tasks. IMC addresses the energy and latency costs of memory accesses dominating AI workloads by transforming conventional memory accesses into ones that compute functions of data in the memory core. As a result, IMC chips have demonstrated at least an order-of-magnitude reduction in the energy-delay product over equivalent von Neumann architectures at iso-accuracy. IMCs also exhibit a fundamental energy vs. SNR trade-off that designers need to exploit to enhance energy efficiency while meeting task-level accuracy requirements. Since its inception in 2014, IMC design has become an active area of research in the integrated circuits and architecture communities. This talk will provide an overview of IMCs, describe various IMC design principles and architectures, review current trends via data-driven extensive benchmarking of IMC chip prototypes, and identify future opportunities and challenges in deploying IMCs at scale in emerging applications.

Naresh R. Shanbhag is the Jack Kilby Professor of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. He received his Ph.D. degree from the University of Minnesota (1993) in Electrical Engineering. From 1993 to 1995, he worked at AT&T Bell Laboratories at Murray Hill where he led the design of high-speed transceiver chipsets for very-high-speed digital subscriber line (VDSL), before joining the University of Illinois at Urbana- Champaign in August 1995. He has held visiting faculty appointments at the National Taiwan University (Aug.-Dec. 2007) and Stanford University (Aug.-Dec. 2014). His research focuses on the design of energy-efficient systems for machine learning, communications, and signal processing, spanning algorithms, VLSI architectures, and integrated circuits. He has more than 200 publications in this area, holds thirteen US patents, and is a co-author of two books and multiple book chapters (see https://shanbhag.ece.illinois.edu/ for details). He received the 2018 SIA/SRC University Researcher Award, became an IEEE Fellow in 2006, received the 2010 Richard Newton GSRC Industrial Impact Award, the IEEE Circuits and Systems Society Distinguished Lecturership in 1997, the National Science Foundation CAREER Award in 1996, and multiple best paper awards. In 2000, Dr. Shanbhag co-founded and served as the Chief Technology Officer of the Intersymbol Communications, Inc., which introduced mixed-signal ICs for electronic dispersion compensation of OC-192 optical links, and became a part of Finisar Corporation in 2007. From 2013-17, he was the founding Director of the Systems On Nanoscale Information fabriCs (SONIC) Center, a 5-year multi- university center funded by DARPA and SRC under the STARnet program. He is currently on the leadership teams of the JUMP 2.0 DARPA and SRC funded Centers for Ubiquitous Connectivity (CUbiC) and Codesign of Cognitive Systems (CoCoSys), and the NSF-industry funded Center for Advanced Semiconductor Chips for Accelerated Performance (ASAP).

Digitally Enhanced Analog Circuits:
Trends & State-of-the-art Designs

Organizer: **Ben Calhoun,** *University of Virginia, Charlottesville, VA*

Co-Organizers: **Visvesh Sathe,** *Georgia Institute of Technology, Atlanta, GA*
                        Jiawei Xu, *Fudan University, Shanghai, China*
                        Jeff Walling, *Virginia Tech, Blacksburg, VA*
                        Masum Hossain, *Carleton University, Ottawa, Canada*
                        Yan Lu, *University of Macau, Macao, China*

Champions: **Makoto Nagata,** *Kobe University, Kobe, Japan*
                        Man-Kay Law, *University of Macau, Macau, China*

Traditional all-analog circuits consume large area, power, and design time in advanced technology nodes and are highly susceptible to process, voltage, and temperature (PVT) parameter variations. Digital circuits with analog functionality or digitally assisted analog circuits help to mitigate these challenges. Digital circuits require less area and power, offer fast time-to-market, provide greater tolerance to PVT variations, and enable critical storage, programmability, and runtime computational capabilities that enhance traditional analog circuits through techniques like calibration and signal processing.

This forum presents the recent treads and state-of-the-art designs for digitally enhanced analog circuits while highlighting the specific circuit components more favorable to digital or analog implementations to improve target metrics in analog, mixed-signal, RF, and power management systems.

Agenda

Time	Topic
Time	**Topic**
8:00 AM	Breakfast
8:15 AM	**Introduction** **Ben Calhoun,** *University of Virginia, Charlottesville, VA*
8:25 AM	**Extending and Augmenting Analog with Digital to Overcome Technology Scaling Limitations** **Alvin Loke,** *NXP, San Diego, CA*
9:15 AM	**Digitally Enhanced Clock Generation and Distribution** **Ping-Hsuan Hsieh,** *National Tsing Hua University, Hsinchu City, Taiwan*
10:05 AM	Break
10:20 AM	**From Microwatts to Terawatts: Managing GPU Power** **Tawfik Rahal-Arabi,** *AMD, Bellevue, WA*
11:10 AM	**Digital and Mixed-Signal ADC Enhancement Techniques** **Pieter Harpe,** *Eindhoven University of Technology, Eindhoven, The Netherlands*
12:00 PM	Lunch
1:20 PM	**Sensitivity and Robustness Enhancement of Ultra-Low Power Digitally Assisted Wakeup Receivers** **Steven Bowers,** *University of Virginia, Charlottesville, VA*
2:10 PM	**Digitally Enhanced Transceiver for High-Speed Signalling** **Charlie Boecker,** *Microsoft, Ames, IA*
3:00 PM	Break
3:15 PM	**Applications of Time-Domain Circuits in SoC's** **Stephen Kosonocky,** *AMD, Fort Collins, CO*
4:05 PM	**Analog Enhanced Digital and Memory Circuits** **Jaydeep Kulkarni,** *University of Texas Austin, Austin TX*
4:55 PM	Closing Remarks

Intelligent Sensing

Organizers: **Kea-Tiong Tang,** *National Tsing Hua University,*
Hsinchu, Taiwan
Mahsa Shoaran, *EPFL, Lausanne, Switzerland*

Co-Organizers: **Rangharajan Venkatesan,** *NVIDIA, Santa Clara, CA*
Marco Berkhout, *Goodix Technology, Nijmegen,*
The Netherlands
Takeshi Sugawara, *The University of*
Electro-Communications, Tokyo, Japan

Champions: **Bruce Rae,** *STMicroelectronics, Edinburgh, United Kingdom*
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*

The forum lies at the interface of sensors and machine learning - including ML architectures for in/near-sensor computing such as biomedical, imaging, environmental, etc. It will cover analog-only architectures, in-memory compute, edge computing, accelerator architectures and technologies that integrate with sensors. The forum will discuss edge compute system tradeoffs in sensor-based applications, system integrations, cloud versus edge computing, and more.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Kea-Tiong Tang,** *National Tsing Hua University, Hsinchu, Taiwan* **Mahsa Shoaran,** *EPFL, Lausanne, Switzerland*
8:25 AM	**Hope for the Best, but Plan for the Worst: Considering Risk and its Mitigation when Designing Intelligent Sensing Systems** **Timothy Denison,** *University of Oxford, Oxford, United Kingdom*
9:15 AM	**Intelligent Imager with Processing-in-Sensor Techniques** **Chih-Cheng Hsieh,** *National Tsing Hua University, Hsinchu, Taiwan*
10:05 AM	Break
10:20 AM	**Activity-Driven Perception for Intelligent Edge Sensory Systems** **Shih-Chii Liu,** *University of Zurich and ETH Zurich, Zurich, Switzerland*
11:10 AM	**Event-Driven Sensory Analog Processing and Massively Parallel Mixed-Signal in-Memory Computing for Distributed Adaptive Intelligence at the Edge** **Gert Cauwenberghs,** *UC San Diego, La Jolla, CA*
12:00 PM	Lunch
1:20 PM	**Cross-Layer Innovations for Enabling Real-Time and Efficient Eye Tracking in VR/AR** **Yingyan Lin,** *Georgia Institute of Technology, Atlanta, GA*
2:10 PM	**Aggressive Design Reuse for Ubiquitous Security - From Design-Time to Run-Time Intelligent Attack Detection and Counteraction** **Massimo Alioto,** *Nat U Singapore, Singapore*
3:00 PM	Break
3:15 PM	**Implementing on-Sensor Machine Learning for Ultralow Power, Always-on Inferencing at the Extreme Edge** **Mahesh Chowdhary,** *STMicroelectronics, Santa Clara, CA*
4:05 PM	**Benefits of System Architecture re-Design for 3D Chiplet Integration Technologies** **Dragomir Milojevic,** *IMEC, Leuven, Belgium*
4:55 PM	Closing Remarks

Recent Developments in High-Performance Frequency Synthesis Circuits and Systems

Organizers: **Masoud Babaie,** *Delft University of Technology, Delft,*
The Netherlands
Wanghua Wu, *Samsung Semiconductor, San Jose, CA*

Co-Organizers: **Jan Prummel,** *Renesas Design Netherlands,*
's-Hertogenbosch, The Netherlands
Wei-Zen Chen, *National Yang Ming Chiao Tung University,*
Hsinchu, Taiwan
Danielle Griffith, *Texas Instruments, Dallas, TX*
Akihide Sai, *Toshiba, Kawasaki, Japan*

Champions: **Matteo Bassi,** *Infineon Technologies, Villach, Austria*
Arun Natarajan, *Oregon State University, Corvallis, OR*

Frequency synthesizers are among the most critical blocks in wireless, wireline, and digital clocking applications. This forum will cover the latest advances in frequency synthesis circuits and systems to efficiently generate LO signals with low phase noise, low spurious tones, and large modulation bandwidth. Prior-art techniques will be discussed in-depth, such as energy-efficient reference clocks, high-FOM wide-tuning range VCOs, low-cost low-power PLLs, and modern fractional-N digital PLLs. Special attention will also be given to pulling and spur mitigation techniques, and injection-locked frequency multipliers. The forum will be concluded by exploring mm-wave PLLs for 5G communication systems, and FMCW generation for high-performance car radars.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Masoud Babaie,** *Delft University of Technology, Delft,* *The Netherlands*
8:25 AM	**Low-Jitter Frequency Generation and Synthesis Utilizing BAW Resonator** **Michael Perrott,** *Texas Instruments, Manchester, NH*
9:15 AM	**Design Techniques to Improve Phase Noise and Tuning Range of Modern RF/mmW Oscillators** **Mina Shahmohammadi,** *NXP Semiconductors, Delft,* *The Netherlands*
10:05 AM	Break
10:20 AM	**Low-Power Fractional-N Digital PLL Design Techniques** **Kenichi Okada,** *Tokyo Institute of Technology, Tokyo, Japan*
11:10 AM	**High Performance Digital Fractional-N PLLs for Connectivity Standards** **Ashoke Ravi,** *Intel, Hillsboro, OR*
12:00 PM	Lunch
1:20 PM	**Design of Advanced Low-Jitter Ring Oscillator-Based ILCMs** **Suneui Park,** *Samsung Electronics, Hwaseong, Korea*
2:10 PM	**Prediction and Mitigation of Spurs in Fractional Synthesizers** **Michael Peter Kennedy,** *University College Dublin, Dublin, Ireland*
3:00 PM	Break
3:15 PM	**DSM Noise Suppression in Analog Frequency Synthesizers: From Low-Power Design to High-Performance mm-Wave Design** **David Murphy,** *Broadcom, Irvine, CA*
4:05 PM	**Linearization Techniques for FMCW Generation in Car Radar Applications** **Luigi Grimaldi,** *Infineon Technologies, Villach, Austria*
4:55 PM	Closing Remarks

Toward Next Generation of Highly Integrated Electrical and Optical Transceivers

Organizers: **Mozhgan Mansuri,** *Intel, Hillsboro, OR*
Jay Im, *AMD, San Jose, CA*

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Peter Ossieur, *Imec, University of Ghent, Ghent, Belgium*
Sudip Shekhar, *University of British Columbia, Vancouver, Canada*
Tamer Ali, *Mediatek, Irvine, CA*

Champions: **Bill Redman-White,** *HiLight Semiconductor, Southampton, United Kingdom*
Yohan Frans, *AMD, San Jose, CA*

The next generation of highly integrated transceivers for high throughput applications poses significant design challenges in terms of power efficiency, signal integrity, ISI and noise cancellation. This forum discusses the key issues for deploying 100G+ SERDES and design approaches for 200G+, including noise mitigation, power efficient analog/digital equalization schemes (CTLE, analog FFE, DSP FFE/DFE/MLSD), modulation, and system integration (packaging, connectors, etc).

Optical transceivers also play a crucial role in extending the reach of electrical interconnects as data rates continue to increase. Various aspects of optical transceivers based on silicon photonics are discussed, such as foundry perspectives, directly modulated vs coherent optical links, packaging techniques and fiber termination challenges. In addition, the forum covers emerging technologies including co-packaged optics and heterogenous integration of both photonic and electronic chiplets, promising denser integration while introducing new challenges.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Mozhgan Mansuri,** *Intel, Hillsboro, OR*
8:25 AM	**Highlights and Challenges in Deploying 100G+ SERDES** **Francis Lin,** *Mediatek, HsinChu, Taiwan*
9:15 AM	**The Impact of Industry Trends on 200+Gbps Wireline R&D** **Tony Carusone,** *Alphawave Semi and University of Toronto, Toronto, Canada*
10:05 AM	Break
10:20 AM	**Beyond 200Gbps Electrical Transceivers – Circuit Architecture, Design Implementation and Silicon-Based Results** **Ariel Cohen,** *Intel, Jerusalem, Israel*
11:10 AM	**Modulation Schemes for Ultra-High-Speed Transceivers** **Naim Ben-Hamida,** *Ciena, Ottawa, Canada*
12:00 PM	Lunch
1:20 PM	**Silicon Photonics Based High Throughput Optical Transceivers** **Mayank Raj,** *AMD, San Jose, CA*
2:10 PM	**Micro-Transfer Printing for Heterogeneous Electronic-Photonic Integrated Circuits** **Gunther Roelkens,** *Ghent University - imec, Ghent, Belguim*
3:00 PM	Break
3:15 PM	**Silicon Photonics and Foundry Requirements for AI Datacenters** **Tom Gray,** *NVIDIA, Durham, NC*
4:05 PM	**Electronic-Photonic Systems-on-Chip for Compute, Communications and Sensing** **Vladimir Stojanovic,** *UC Berkeley, Berkeley, CA*
4:55 PM	Closing Remarks

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*To a life well lived

Kenneth C. Smith

*ISSCC volunteer since 1974 in various roles:
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COVID 19 PROTOCOLS

The health and safety of our conference attendees is our top priority. The ISSCC 2024 conference Organizing Committee remains vigilant in monitoring the COVID-19 pandemic. The conference will follow CDC and State of California guidelines. ISSCC is planned as an in-person event but it also has an online offering. We look forward to you joining us in San Francisco, CA. If you don't feel comfortable participating in large gatherings, or if your organization has travel restrictions, we encourage you to join us online.

MASKS, VACCINATION, SANITIZERS

Masks help slow the spread of the virus. They help to protect the medically vulnerable and those unable to get vaccinated. In San Francisco there are no longer masking requirements for most people. People may choose to wear masks, even when they are not required. Respect the choices others make for their health.

Currently, proof of vaccination is no longer required in meetings in San Francisco. We will be monitoring that regulation and the ISSCC website will be updated as regulations change.

Hand sanitizing lotion will be available throughout the hotel and at the Registration desk.

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Saturday, February 17:	4:00 pm to 7:00 pm
Sunday, February 18:	7:00 am to 8:30 pm
Monday, February 19:	6:30 am to 4:00 pm
Tuesday, February 20:	8:00 am to 4:00 pm
Wednesday, February 21:	8:00 am to 4:00 pm
Thursday, February 22:	7:00 am to 2:00 pm

Students must present their Student ID
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Deadlines: The deadline for registering at the Early Registration rates is 12:00 Midnight EST **Sunday January 14, 2024.** After January 14th, and before 12:00 Midnight EST **Monday January 29th, 2024,** registrations will be processed **at the Late Registration rates. After January 29th, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments: Prior to 12:00 Midnight EST **Monday January 29, 2024,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments.

No refunds will be made after 12:00 Midnight EST January 29th, 2024. Paid registrants who do not attend the conference will have access to the on-demand material.

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-Keep up with the latest trends and cutting-edge developments in our industry - through our electronic newsletters, member magazine "Solid-State Circuits Magazine", and our award winning "Journal of Solid State Circuits".

-Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and members-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

-Connect with your Peers - valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.

-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.

-Access publications and EBooks - discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world's technical research to keep your knowledge current. Publications included in your SSCS membership are the "RFIC Virtual Journal" (RFVJ) and the "Journal on Exploratory Solid-State Computational Devices and Circuits" (JxCDC), Solid State Letters, and our newest Journal, the "Open Journal of the Solid-state Circuits Society" (OJ-SSCS) a fully open-access publication.

SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will again receive an exclusive benefit of a $30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuits Society today at sscs.ieee.org - you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions & more: In person registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. Access to author interviews, social hours, to the Student Research Preview, to the Demo Sessions, to the open Women in Circuits Programs and to the new Exhibition are also included. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from 3:00 pm to 8:00 pm; on Tuesday from 9:30 am to 1:30 pm; on Tuesday from 3:00 pm to 8:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Exhibition: For the first time in 2024, ISSCC is planning to organize an Exhibition open to Companies and non-academic Research Institutions. The main aim of the Exhibition is to showcase the participating Corporations/Institutions, their products and their applications. The Exhibition will be open on Monday from 3:00 pm to 8:00 pm; on Tuesday from 9:30 am to 1:30 pm; and on Tuesday from 3:00 pm to 8:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Monday and Tuesday Social Hours: Refreshments will be available starting at 5:30 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

Publications: All ISSCC registrants will be able to access online the Digital Digest and the registrations of the Technical Presentations Besides, Conference registration includes:

-Papers Visuals: The visuals from all papers presented will be available by download.

-Demonstration Session Guidebook: A descriptive guide to the Demonstration Session will be available by download.

-Note: Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course include breakfast, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times.

CONFERENCE INFORMATION

OPTIONAL PUBLICATIONS

ISSCC 2024 Publications: The following ISSCC 2024 digital publications can be purchased in advance or on site:

2024 ISSCC Download USB: All of the downloads included in conference registration, (regular papers and presentations) **(mailed in March)**

2024 Tutorials USB: All of the 90 minute Tutorials **(mailed in June).**

2024 Short Course USB: (mailed in June).

The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration website can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. ***Conference room rates are $279 for a single/double (per night plus tax).*** In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free.** All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. **Telephone:** Call 877- 622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2024 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 29th, 2024 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 29th, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

IEEE NON-DISCRIMINATION POLICY

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.

EVENT PHOTOGRAPHY

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REFERENCE INFORMATION

Conference Website:	www.isscc.org	
ISSCC Email:	ISSCC@ieee.org	
Registration questions:	ISSCCinfo@yesevents.com	
Hotel Information:	San Francisco Marriott Marquis 780 Mission Street San Francisco, CA 94103	Phone: 415-896-1600
Press Information:	Laura C. Fujino University of Toronto Email: lcfujino@aol.com	Phone: 416-418-3034
Registration:	YesEvents PO Box 3024 Westminster, MD 21158 Email: issccinfo@yesevents.com	Phone: 800-937-8728 Fax: 410-559-2236

Hotel Transportation
Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links. You can get a map and driving directions from the hotel website at:
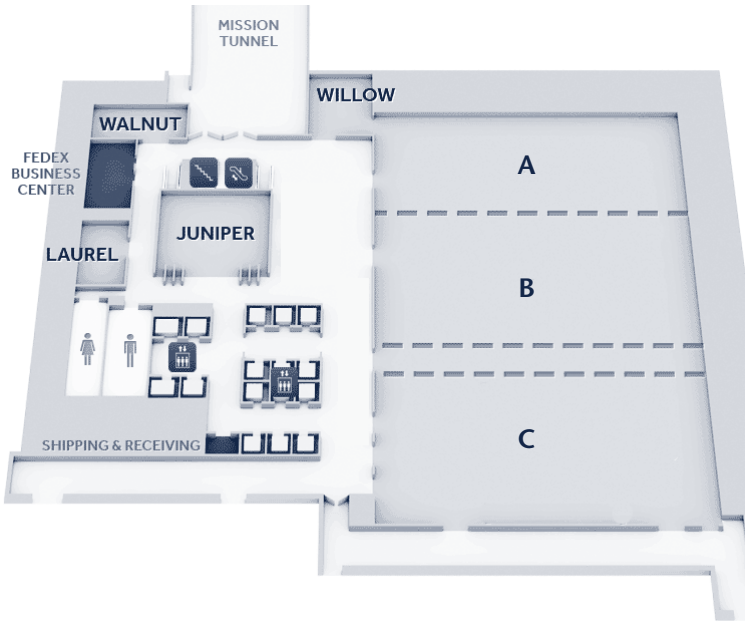www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location:
ISSCC 2025 will be held on February 16-20, 2025
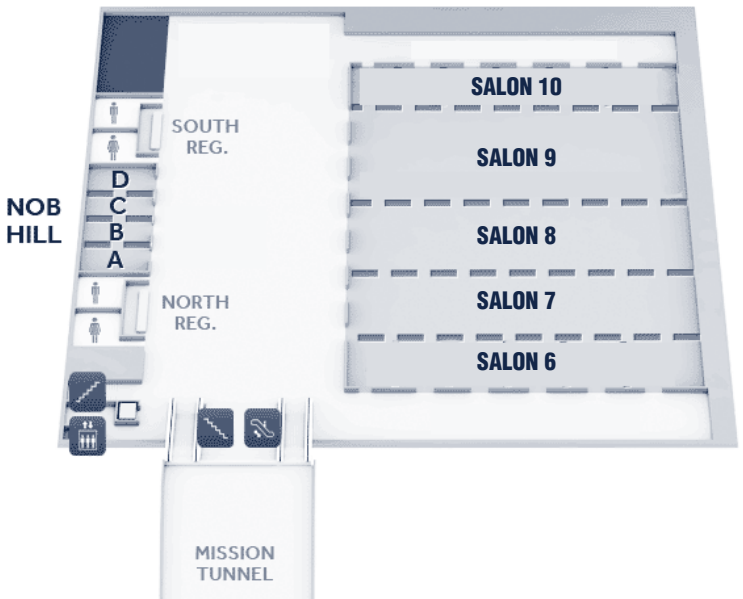at the San Francisco Marriott Marquis Hotel.

SUBCOMMITTEE CHAIRS

Analog:	Maurits Ortmanns
Data Converters:	Jan Westra
Digital Architectures & Systems:	Rahul Rao
Digital Circuits:	Keith Bowman
Imagers, MEMS, Medical & Displays:	Rikky Muller
Memory:	Meng-Fan Chang
Power Management:	Bernhard Wicht
RF:	Brian Ginsburg
Security:	Ingrid Verbauwhede
Technology Directions:	Ali Hajimiri
Wireless:	Chih-Ming Hung
Wireline:	Thomas Toifl

Program-Committee Chair:	Frank O'Mahony
Program-Committee Vice-Chair:	Thomas Burd
Conference Chair:	Eugenio Cantatore

B2 LEVEL
GOLDEN GATE HALL

MISSION TUNNEL

WILLOW

WALNUT

FEDEX BUSINESS CENTER

JUNIPER

LAUREL

A

B

C

SHIPPING & RECEIVING

LOWER B2 LEVEL
YERBA BUENA BALLROOM

SOUTH REG.

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445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

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